

Introduction to Digital Electronics

Introduction

- Electronics has been an important part of engineering and science world as well as a normal human being from the mid twentieth century.
- Electronics deals with flow of current, but this current flow is due to a controlled flow of electrons (or charge carriers, to be generic) in gas or vacuum in early stages to solid state semiconductors in modern devices.
- In fact, the major breakthrough in the field of electronics is the use of Semiconductor materials, which made electronic circuits and devices small, cheap, reliable and consume very low power.
- Electronics circuits can be divided into two broad categories, digital and analog.
- Analog electronics involves quantities with continuous values.
- Digital electronics involves quantities with discrete values (0,1). The discrete values are achieved by using switching (transistor, diode).

Binary Digits

[0,1] are the two digits in the binary system which called bit.

0	1	0= no voltage
Low	High	1= full source voltage
OFF	ON	0= low voltage < 1V
False	True	1=high voltage >4V

Two system are presented

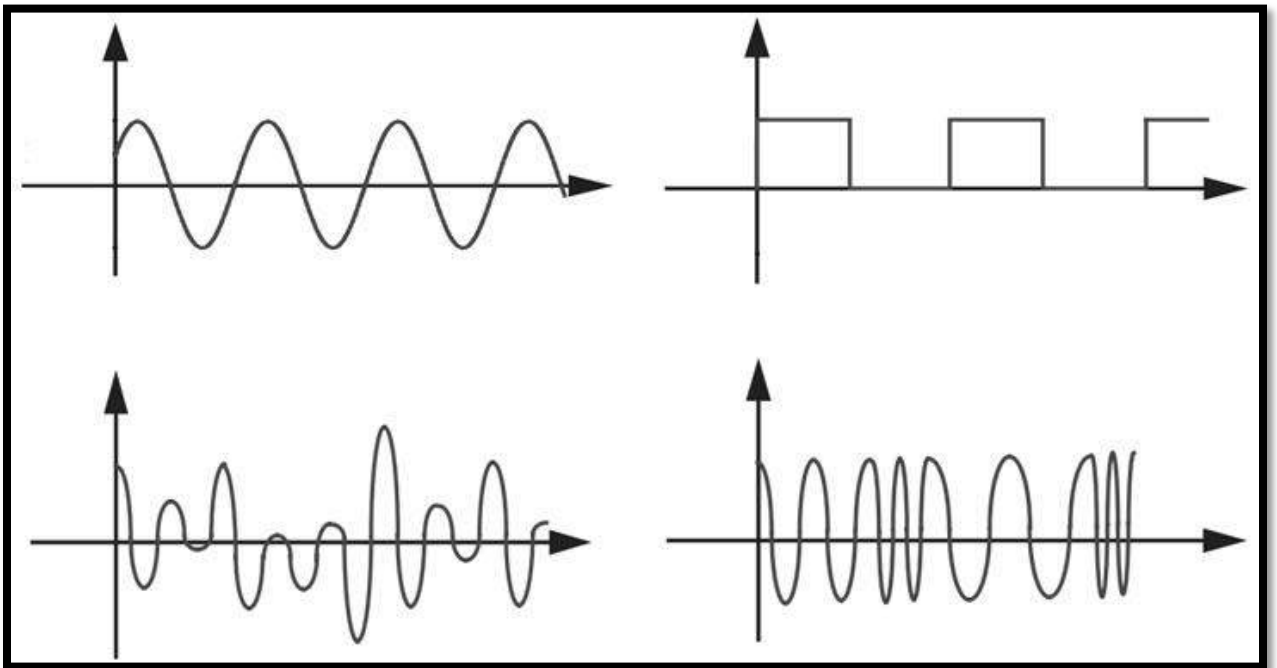
Positive logic
HIGH = 1 (+10V)
LOW = 0 (+2V)

Negative logic
HIGH = 0 (-2V)
LOW = 0 (-10V)

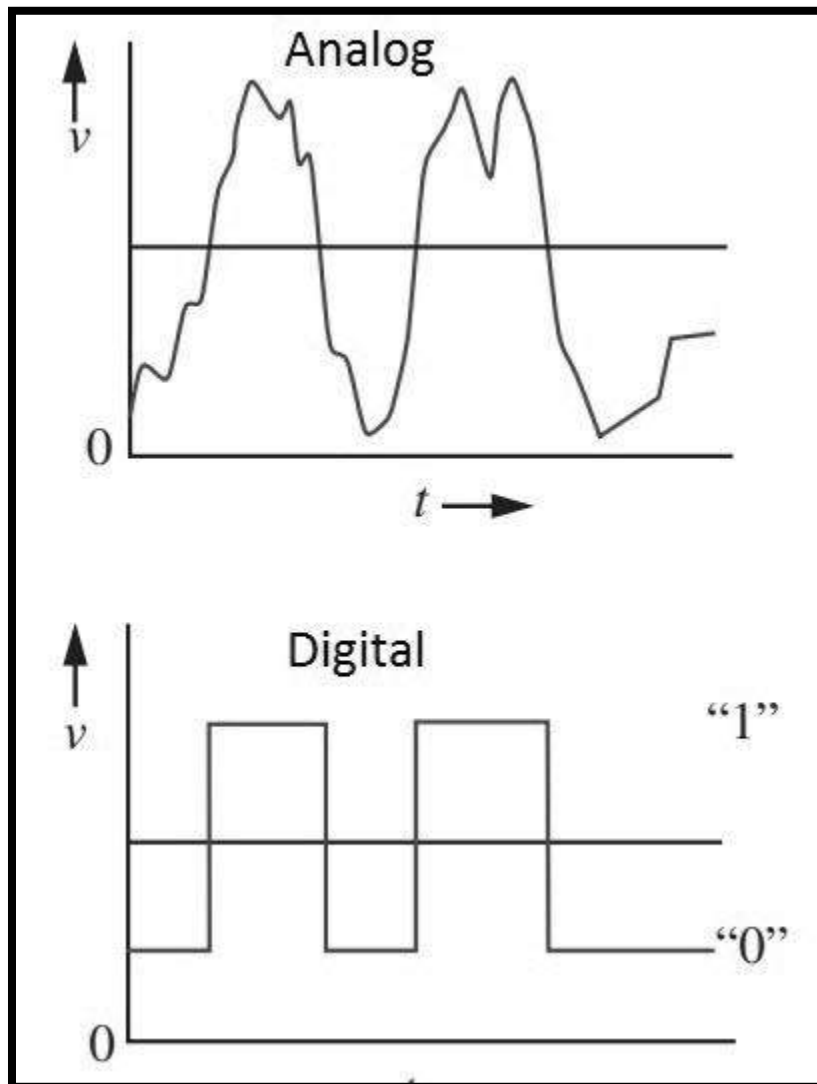
- Groups of bits called CODES which represent number, symbols, instructions..

- **Analog Signals and Digital Signals**

- Almost all the signals in the World are analog i.e. they are continuously varying values. There is lot of continuously variable signals or simply analog signals in nature like light, motion, sound, temperature, pressure etc.
- The following image shows typical analog signals.

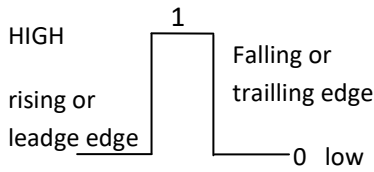
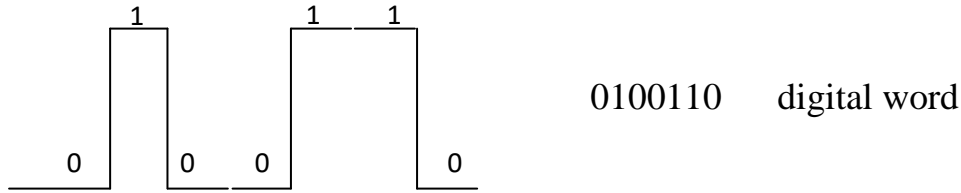


- Digital Signals vary in discrete levels, in contrast to the continuous representation of analog signals. Generally, the discrete levels in a digital signal are just two values: ON and OFF. Even though all the physical signals of the nature are continuous analog signals, representing signals as discrete values has its own advantages.

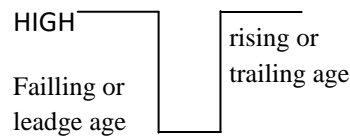


Digital Waveforms

A digital waveform is made up of a series of pulses.



(a) Pulse-positive



(b) Pulse-negative

Logic Gates

A logic gate is an electronic circuit which makes logic decision. In an electronic digital system, the instructions have to be converted into electrical signals. It has one output and one or more inputs. The output signal appears only for certain combinations of input signals.

Logic gates \equiv building blocks

To express the logic operations of a gate the truth table lists all inputs and outputs

$$N=2^n$$

No. of possibilities = n

(N) combinations = 2

Where (n) is the number of inputs

$$n = 2 \quad N=4$$

$$n = 3 \quad N=8$$

$$n = 4 \quad N=16 \text{ and so on}$$

LOGIC GATES

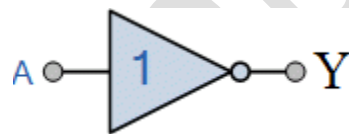
Logic gates: are physical devices which perform logic operation on one or more logical inputs, and produces a single logical output.

There are three groups of logic gates

- 1- Basic gates : NOT, AND and OR
- 2- Universal gates: NAND and NOR
- 3- Arithmetic gate: XOR and XNOR

1- NOT –Gate

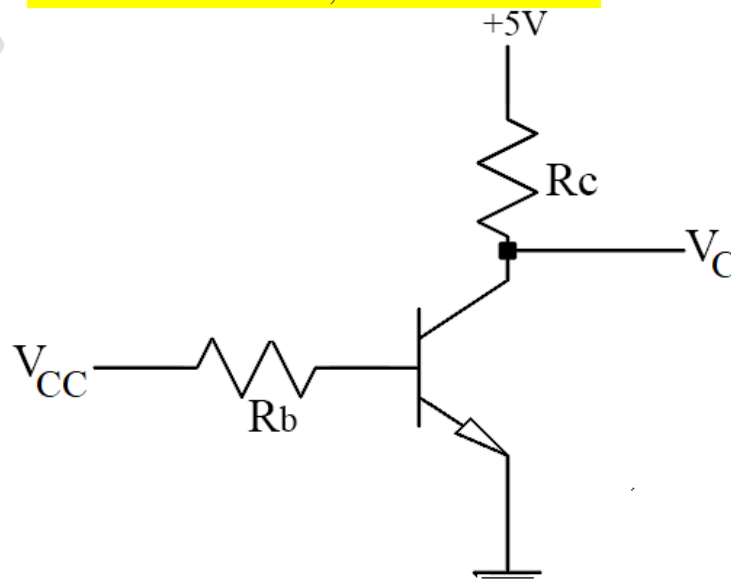
It is also known as an inverter because the output is opposite to the input. It has one input and one output. Circuit diagram of NOT gate using transistor is shown below:



Its Boolean equation is

$$\bar{A} = Y$$

“If A is NOT HIGH, then Y is HIGH”



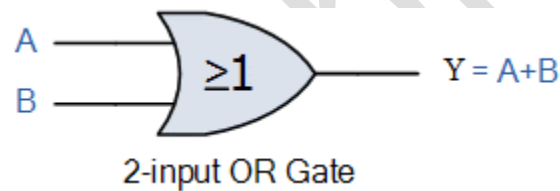
$$V_{CC} = I_C R_L + V_{CE} = I_C R_L + V_C$$

$$X = I_C R_L + Y$$

- When $X=0$
- Low voltage level at the base of the transistor, the transistor will be cutoff, $I_C = 0$ so $I_C R_L = 0$ and $Y = V_{CC} = 1$ (high voltage level)
- When $X=1$
- High voltage level at the base of the transistor, the transistor will be ON, and $I_C = I_C(\text{sat.})$ so $I_C R_L = V_{CC}$ that leaves Y a low voltage level $Y=0$ (low voltage level).

2- OR-Gate

An OR-gate has two or more inputs but only one output.

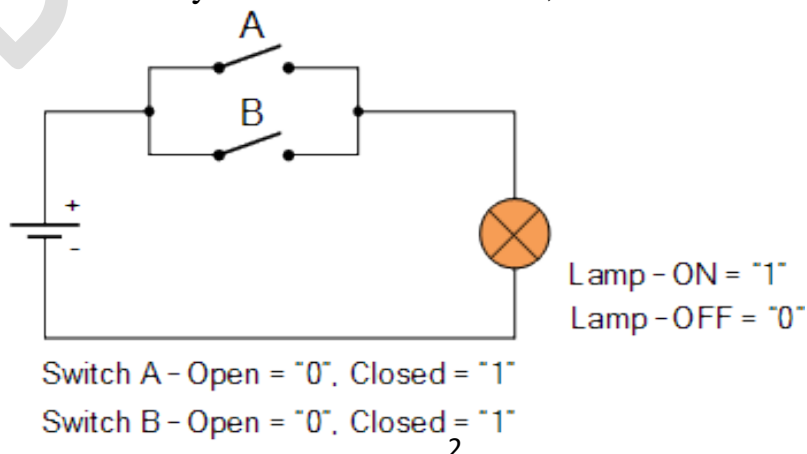


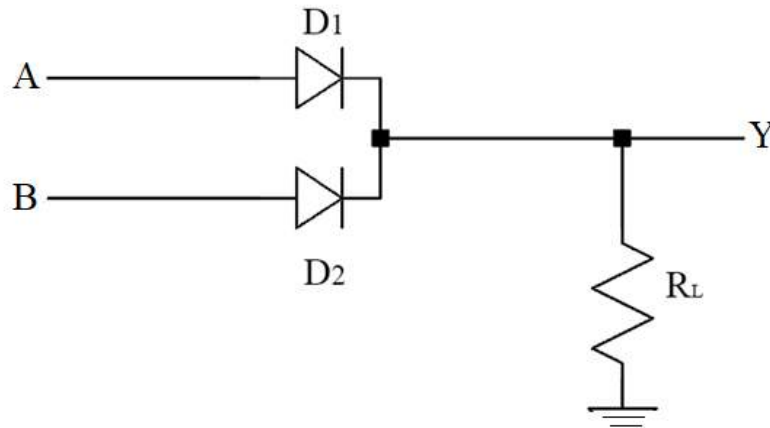
The Boolean equation of this gate is

$$A+B=Y \text{ (A or B)}$$

If A or B is HIGH, then Y is HIGH

In an electrical system, a 2-input OR gate is equivalent to two switches in parallel. When any of the switches are on, the circuit is on.





- If all inputs are in LOW, both diodes are reverse biased hence acts as an open switch. Hence the output voltage is 0V.
- If A is HIGH and B is LOW, diode D_1 becomes forward biased hence act as the closed switch. While D_2 is reverse biased so it acts as an open switch. Hence the output is HIGH.
- Also, If A is LOW and B is HIGH. Diode D_2 is forward biased and acts as an open switch. Diode D_1 is reverse biased and so it acts as an open switch. Hence the output is HIGH.
- If both input are HIGH, the two diodes are forward biased, they act as closed switches and so the output will be HIGH.

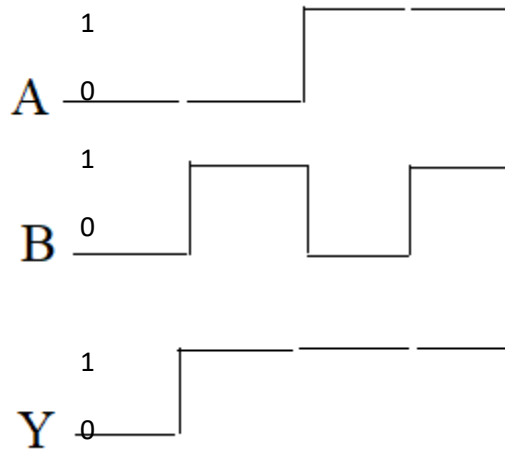
No. of combinations $=2^n$,

$$2^2=4$$

Truth Table

A (2^1)	B (2^0)	Y	Description
0	0	0	A and B are both open, lamp OFF
0	1	1	A is open and B is closed, lamp ON
1	0	1	A is closed and B is open, lamp ON
1	1	1	A is closed and B is closed, lamp ON

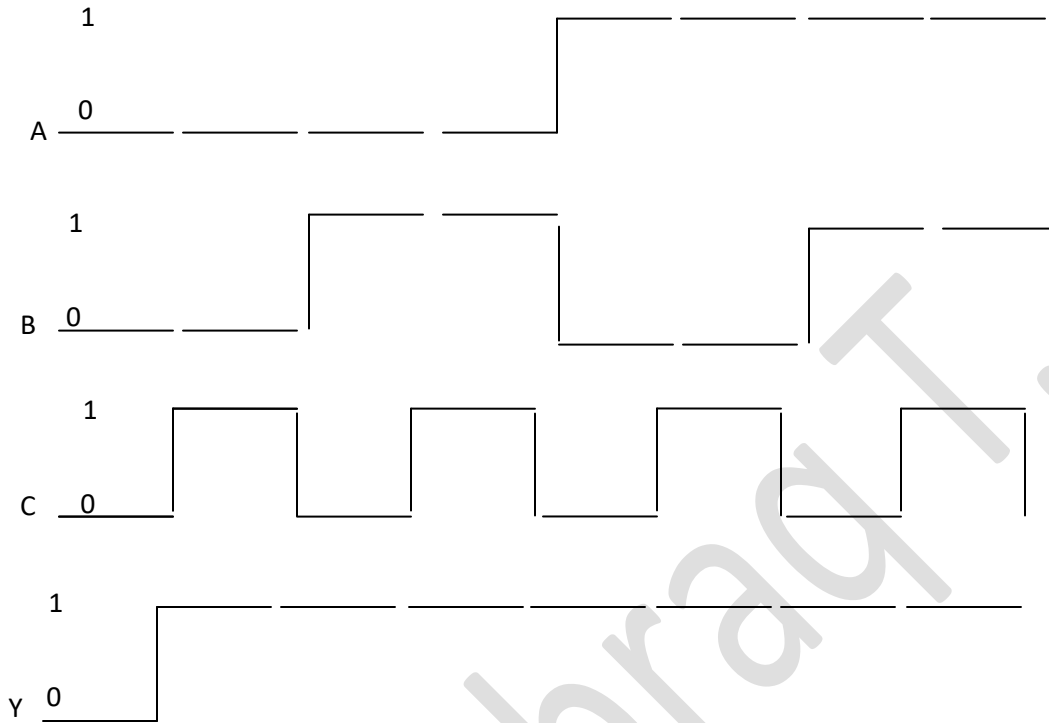
Pulse Duration



Truth table for 3-inputs: it has $2^3=8$ combinations

A (2^2)	B (2^1)	C (2^0)	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Pulsed Operation



3- AND-Gate

An AND- gate has two or more inputs but only one output.



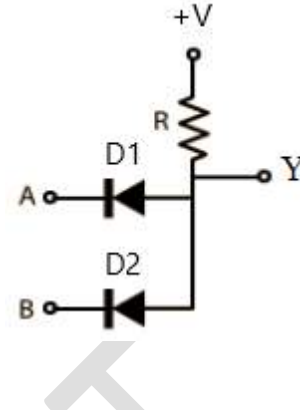
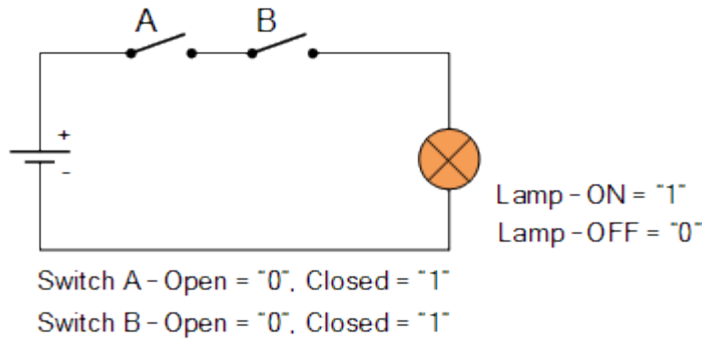
Its Boolean equation is

$$A \cdot B = Y, \text{ A and B} = Y$$

“If both A and B are HIGH, then Y is HIGH”

In an electrical system, a 2-input AND- gate is equivalent to two switches in series. When the two switches are on, the circuit is on.

Lecture Two



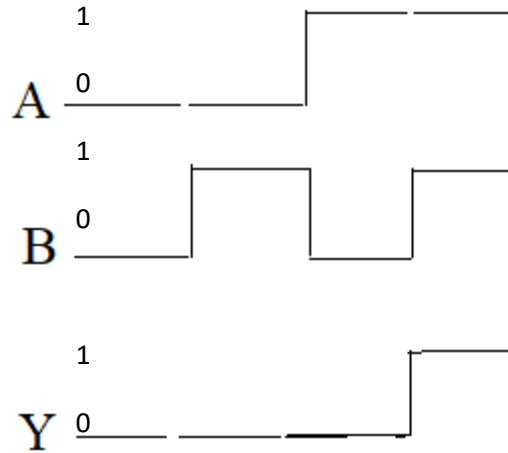
- If A is HIGH and B is LOW, the diode D_1 is reversed biased hence act as an open switch, diode D_2 is forward biased hence act as the closed switch. Hence the output is LOW.
- If A is LOW and B is HIGH, the diode D_1 is forward biased hence act as a closed switch, diode D_2 is reversed biased hence act as an open switch. The output is LOW.
- If all inputs are 0 then both diodes are forward biased and act as closed switch. Hence the output is LOW.
- When both inputs are HIGH then both diodes are reversed biased hence act as an open switches. Hence the output is HIGH.

No. of combinations = 2^n , $2^2=4$

Truth Table

A (2^1)	B (2^0)	Y	Description
0	0	0	A and B are both open, lamp OFF
0	1	0	A is open and B is closed, lamp OFF
1	0	0	A is closed and B is open, lamp OFF
1	1	1	A is closed and B is closed, lamp ON

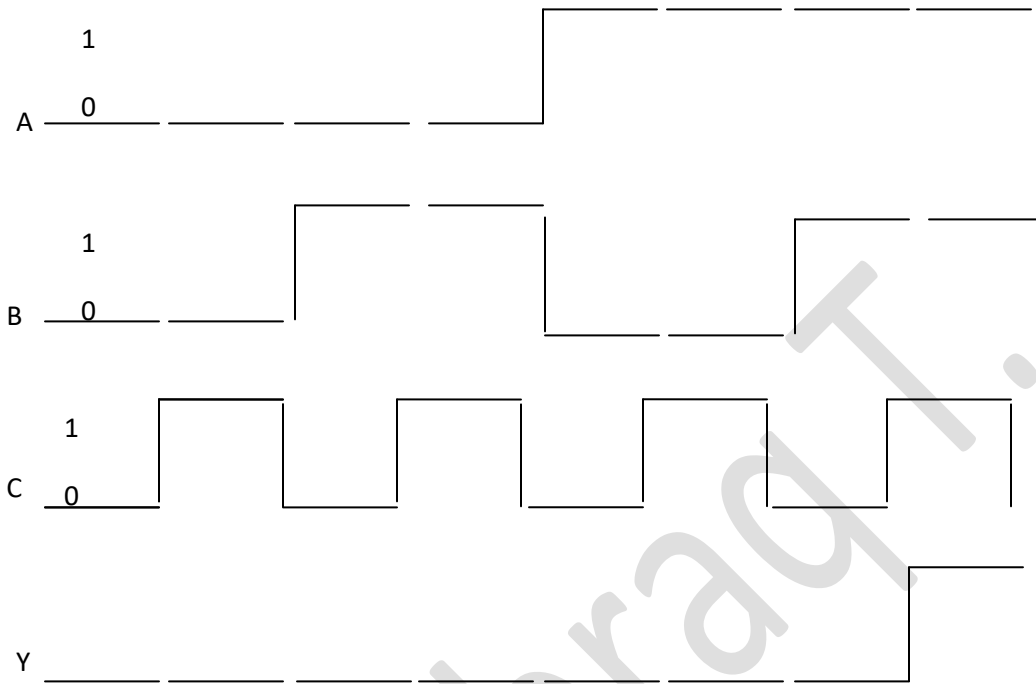
Pulse Duration



Truth table for 3-inputs: it has $2^3=8$ combinations

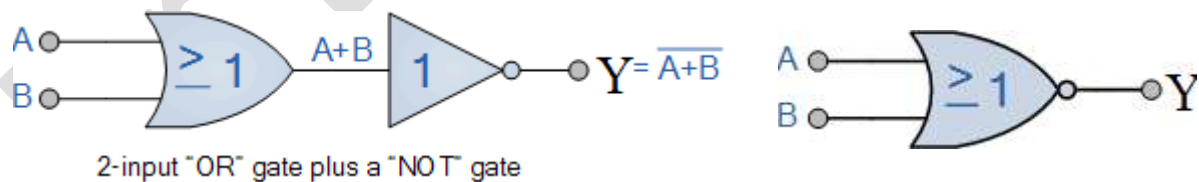
A (2^2)	B (2^1)	C (2^0)	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Pulse Duration



4- NOR-Gate

A NOR gate is a combination of OR gate and NOT gate, it is NOT-OR, i.e. an OR function with an inverted output. It has two or more input signals but only one output signal. All input must be low to get a high output.



Its Boolean equation is

$$Y = \overline{A + B}$$

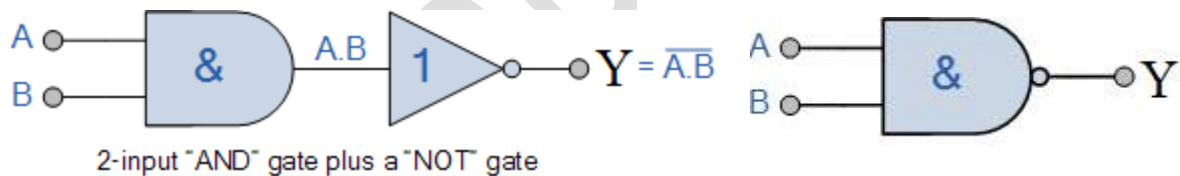
“If both A and B are NOT true, then Y is true”

Logic Operation: A low output occurs when any of its inputs are high. Only when all the inputs are low is the output high.

A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

5- NAND-Gate

A NAND gate is a combination of AND gate and NOT gate (NOT-AND) i.e. an AND operation with an inverted action. It has two or more input signals but only one output signal.



Its Boolean equation is

$$Y = \overline{A.B}$$

If both A and B are HIGH, then Q is NOT HIGH

Logic operation: a low output occurs only when all inputs are high. If any of the inputs are low, the output will be high.

Truth table

A	B	A.B	$\overline{A.B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Parity

Even parity: a logic word with an even no's of 1's

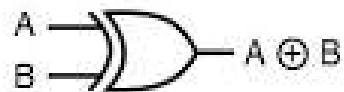
11, 11011, 10111

Odd parity: a logic word with an odd no's of 1's

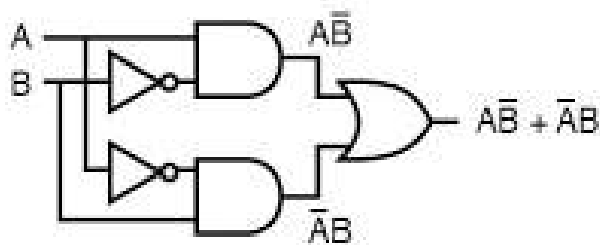
111, 1101

6- XOR-Gate (Exclusive OR gate)

An exclusive OR gate recognizes words which have an odd number of ones.



... is equivalent to ...



$$A \oplus B = A\bar{B} + \bar{A}B$$

Its Boolean equation

$$Y = \bar{A}B + A\bar{B} = A \oplus B$$

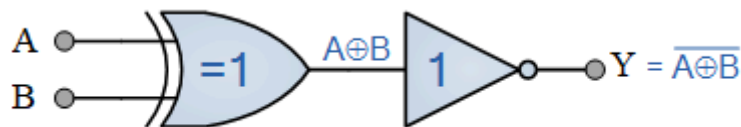
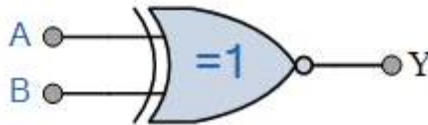
“A OR B but NOT both”

Truth Table N=4

A	B	\bar{A}	\bar{B}	$A\bar{B}$	$\bar{A}B$	$\bar{A}B + A\bar{B} = A \oplus B$
0	0	1	1	0	0	0 even parity
0	1	1	0	0	1	1 odd parity
1	0	0	1	1	0	1 odd parity
1	1	0	0	0	0	0 even parity

7- XNOR (Exclusive-NOR gate)

XOR- followed by an inverter NOT-XOR. It recognizes even parity words.



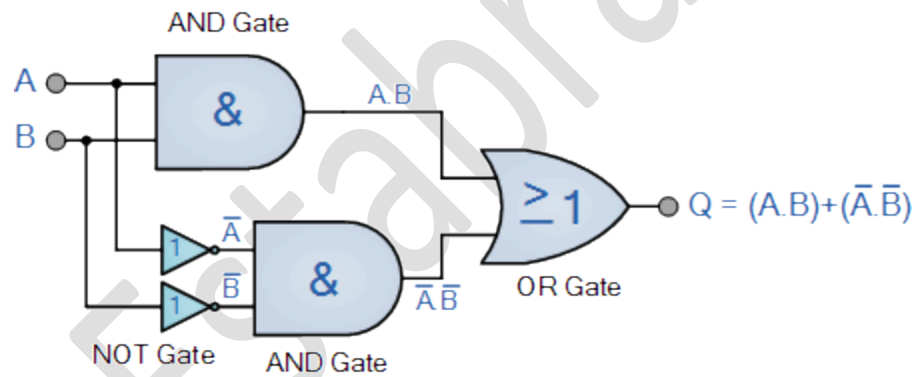
2-input "Ex-OR" gate plus a "NOT" gate

Lecture Two

Its Boolean equation

$$Y = \overline{A} \oplus \overline{B} = (A \cdot B) + (\overline{A} \cdot \overline{B})$$

A	B	\overline{A}	\overline{B}	$A\overline{B}$	$\overline{A}B$	$\overline{A}B + A\overline{B}$	$\overline{\overline{A}B} \oplus \overline{A\overline{B}}$
0	0	1	1	0	0	0	1
0	1	1	0	0	1	1	0
1	0	0	1	1	0	1	0
1	1	0	0	0	0	0	1

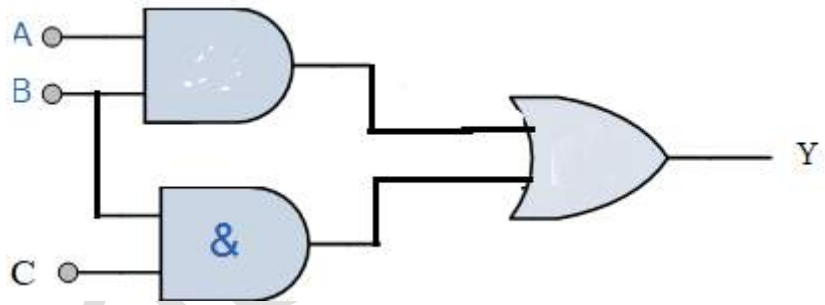


1- Combinational Circuits

A combinational circuit is the digital logic circuit in which the output depends on the combination of inputs at that point of time with total disregard to the past state of the inputs.

Example 1: Give the logic equation for the given logic circuits and give the truth table

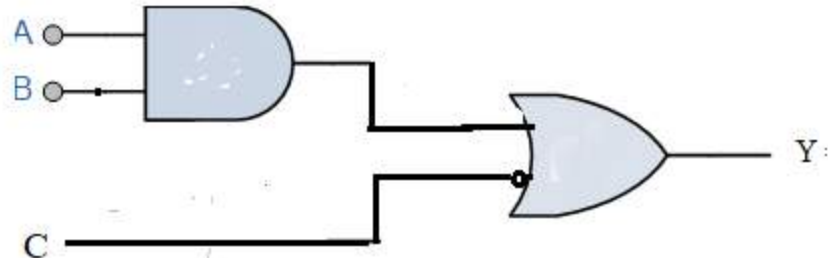
$$Y = AB + BC$$



$$Y = A.B + B.C$$

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

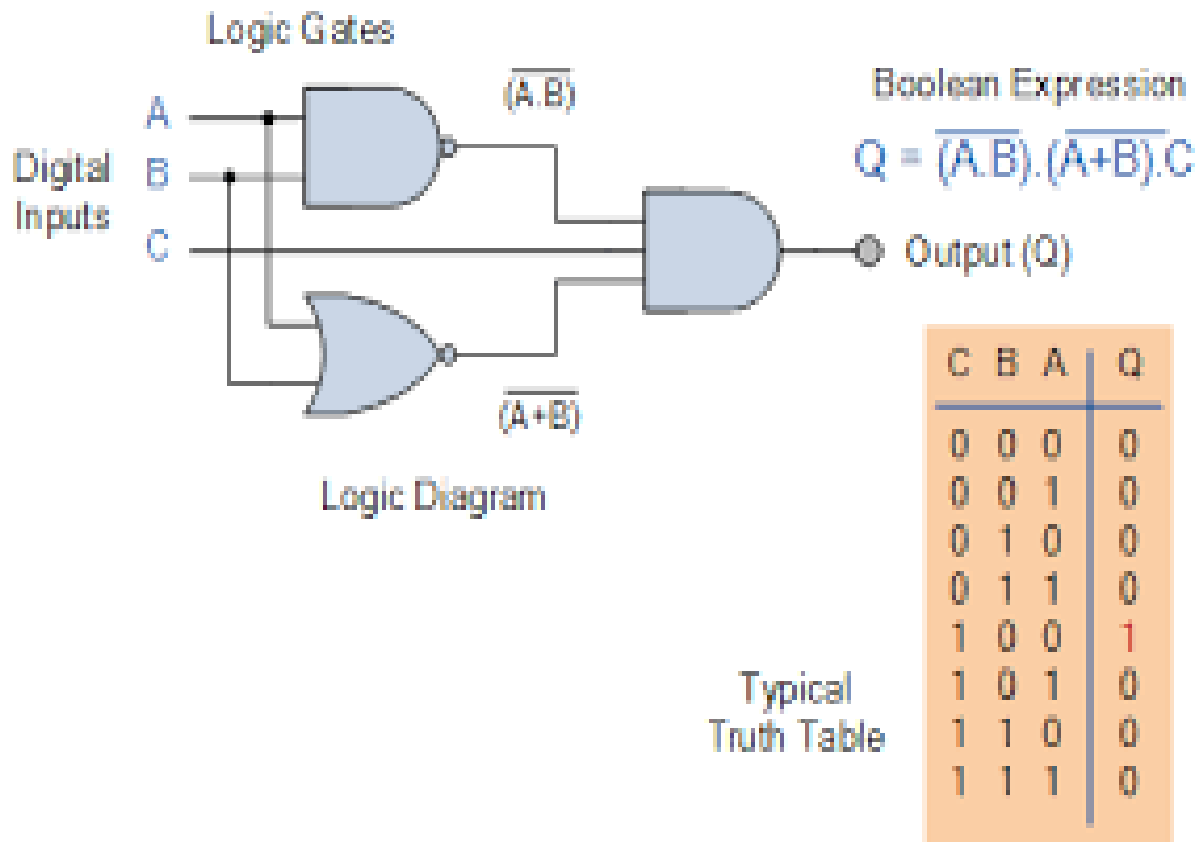
Example 2: Give the logic equation for the given logic circuits and give the truth table



$$Y = A \cdot B + \bar{C}$$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Example 3: Give the logic equation for the given logic circuits and give the truth table



2- Applications

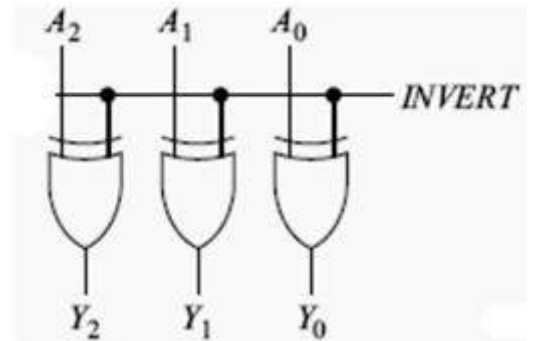
2-1 Controlled Inverter

This is inverter with 3-bit register.

Low inverter ($y=0$) $\implies A_2A_1A_0=y_2y_1y_0$

High inverter ($y=1$) $\implies A_2A_1A_0=\bar{y}_2\bar{y}_1\bar{y}_0$

This circuit can transmit the register contents or the 1's complement of the register contents.



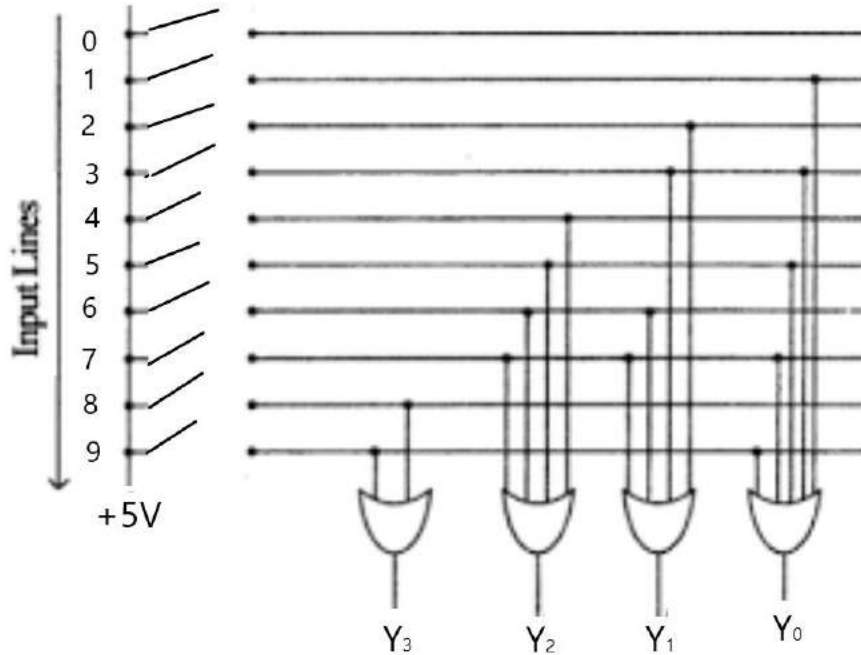
Low INVERTER $y_n=A_n$

High INVERTER $y_n=\bar{A}_n$

It's used in solving arithmetic and logic problems.

2-2 decimal-to-binary encoder

The output number is the binary number equivalent to the decimal number of the closed switch, i.e. if switch no.4 is closed the output number is the binary number of 4.



When key 1 is pressed	$y_2y_1y_0=001$
When key 2 is pressed	$y_2y_1y_0=010$
When key 3 is pressed	$y_2y_1y_0=011$
When key 4 is pressed	$y_2y_1y_0=100$
When key 5 is pressed	$y_2y_1y_0=110$
When key 6 is pressed	$y_2y_1y_0=111$

2-3 Binary to Decimal Decoder

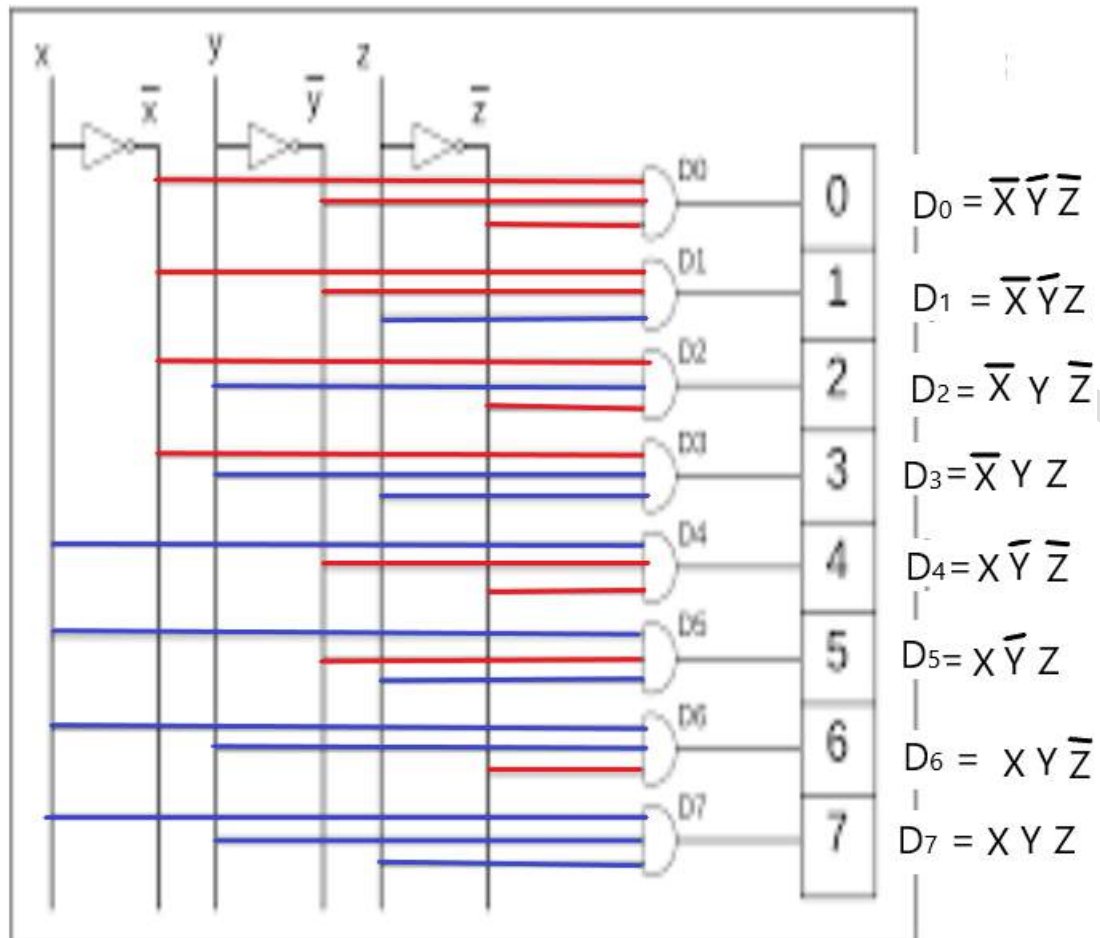
The input number is a binary. Its decimal equivalent is the number assigned to the AND-Gate whose output will be 1.

All inputs for this AND gate are high so the output high

XYZ= 101 $D_5=ON$ 101=5

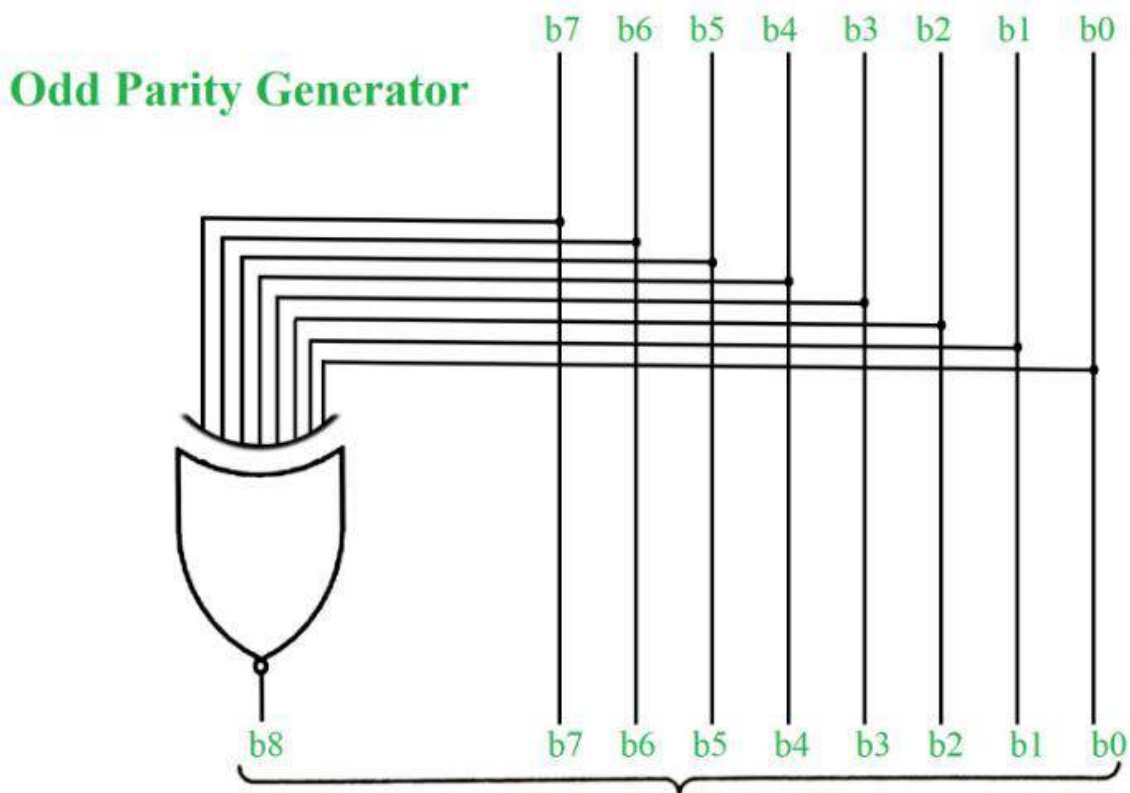
ABC= 100 $y_4= ON$ 100=4

Since only 1 of 5 output lines has a high voltage



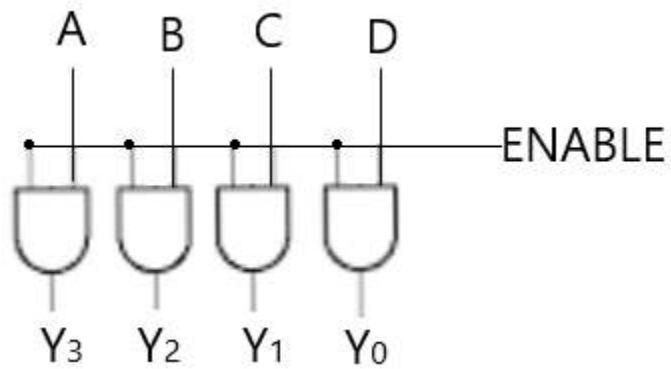
2-4 Odd parity generators

The **odd parity generator** maintains the binary data in an **odd** number of 1's, for example, the data taken is in even number of 1's, this **odd parity generator** is going to maintain the data as an **odd** number of 1's by adding the extra 1 to the even number of 1's. So 1 is added to the real even no. to change it to odd parity.



- If $b_0b_1b_2b_3b_4b_5b_6b_7$ is a number of odd parity, the output of the XNOR-Gate is 0 i.e. $b_8 = 0$ and the output will be the same as the input, of odd parity.
Input number = 1110101(odd parity)
Output number = 01110101(odd parity)
- If $b_0b_1b_2b_3b_4b_5b_6b_7$ is a number of even parity, the output of the XNOR-Gate =1 i.e. $b_8=1$ and the 1 will be added to the output number. This means that a 1 will be added to the input even number, making the number of 1's odd ,odd parity.
Input number = 1100110(even parity)
Output number=11100110 (odd parity)

3- bit Register



- When ENABLE=0 all AND-Gates are disabled.
 $Y_3Y_2Y_1Y_0=0000$ (no matter what the register content).
- When ENABLE=1 the output of the AND-GATE will be according to the second input on each gate.
 $Y_3Y_2Y_1Y_0 = ABCD$ (the output of each gate depends on the data inputs)

Arithmetic Logic Circuits

1- Addition

- There are many information-processing tasks performed by the digital computer, which include arithmetic operations.
- The most basic arithmetic operation is the addition of two binary digits.
- The simple-addition consists of four-possible elementary operations.

$$0+0=0$$

$$0+1=1$$

$$1+0=1$$

$$1+1=10 \text{ [0 with carry 1]}$$



- A combinational circuit that performs the addition of two bits is called a **half-adder** and the one which performs the addition of three bits is called a **full-adder**.

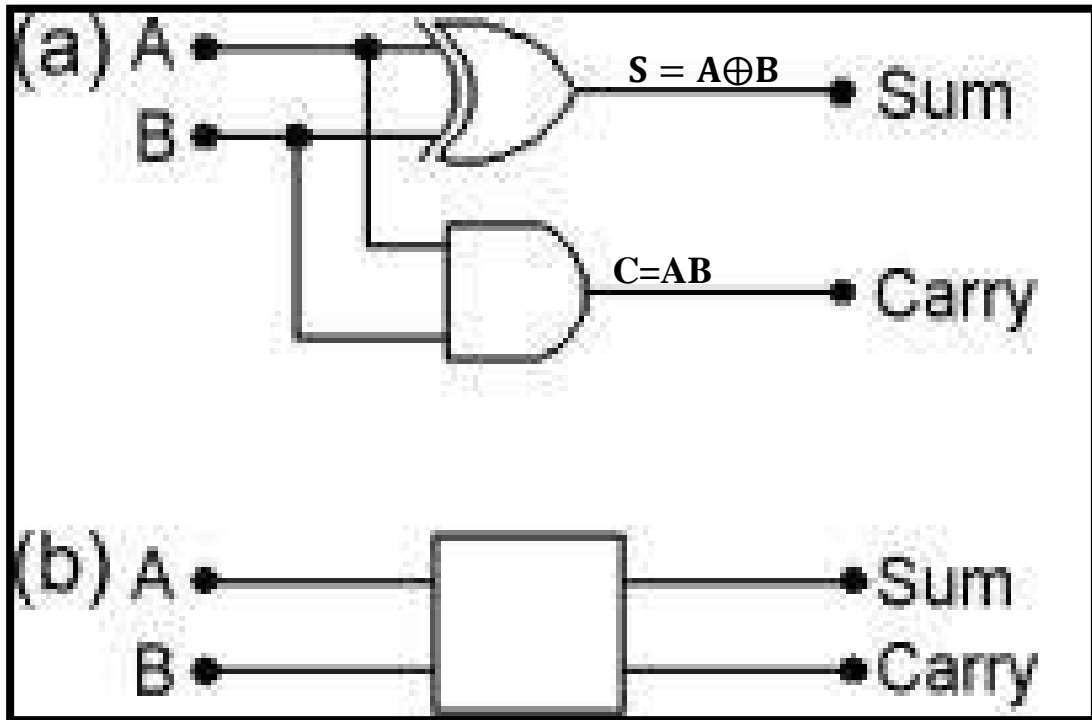
1-1 The Half- Adder

- The half adder is a logic circuit that performs the addition of two binary bits. The inputs to the circuit are two bits, say A and B, and the outputs of the circuits **Carry** and **Sum**, denoted by **C** and **S** separately.
- The sum (or S) is 1 when A and B are different and the carry (or C) is a 1 A and B are 1s.

$$S = A \oplus B$$

$$C = AB$$

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



1-2 The Full- Adder

- A full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs.
- Two of the input variables, denoted by A and B, represented the two significant bits to be added.
- The third input, C_0 , represents the carry from the previous lower significant position. The two outputs are designed by the symbols S and C for carry.
- The binary variable S gives the value of the least significant bit of the sum. The binary variable C gives the output carry.

$$S = A \oplus B \oplus C$$

$$C_0 = AB + BC + AC$$

Lecture 5

Inputs			Outputs		
A	B	C	S	C _o	
0	0	0	0	0	
0	0	1	1	0	
0	1	0	1	0	
0	1	1	0	1	
1	0	0	1	0	
1	0	1	0	1	
1	1	0	0	1	
1	1	1	1	1	

- When all inputs bits are 0's, the output is 0.
- The S output is equal to 1 when only one input is equal to 1 or when all three inputs are equal to 1.
- The C_o output is equal to 1 when two inputs are equal to 1.

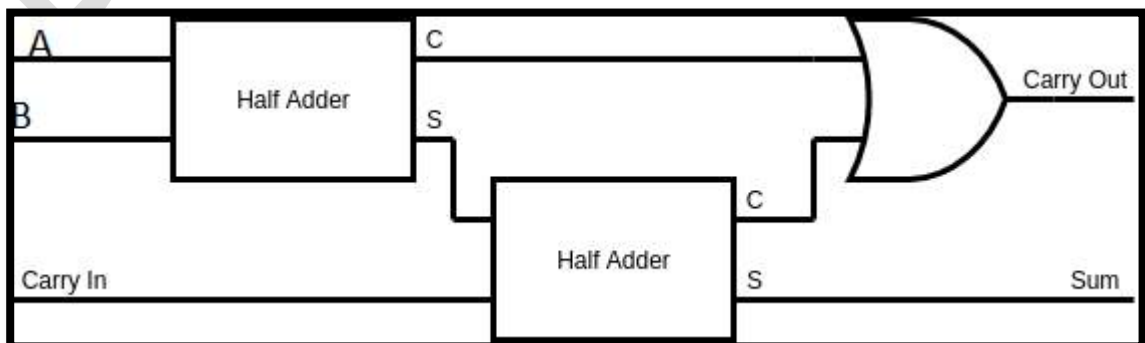
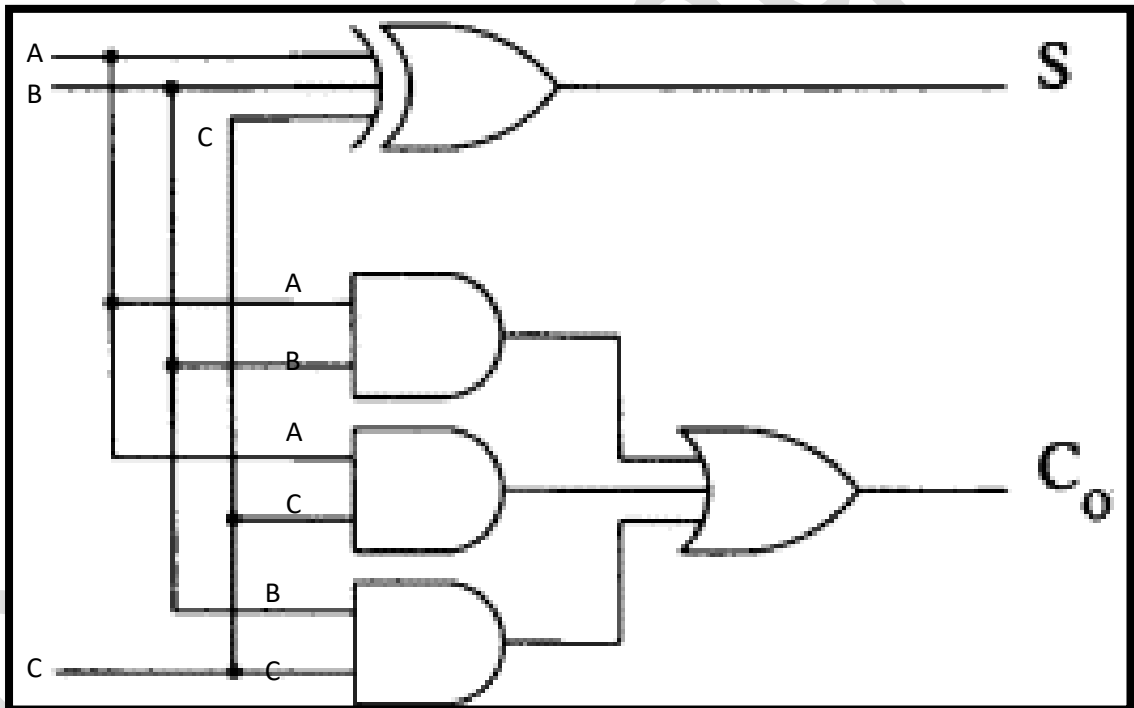
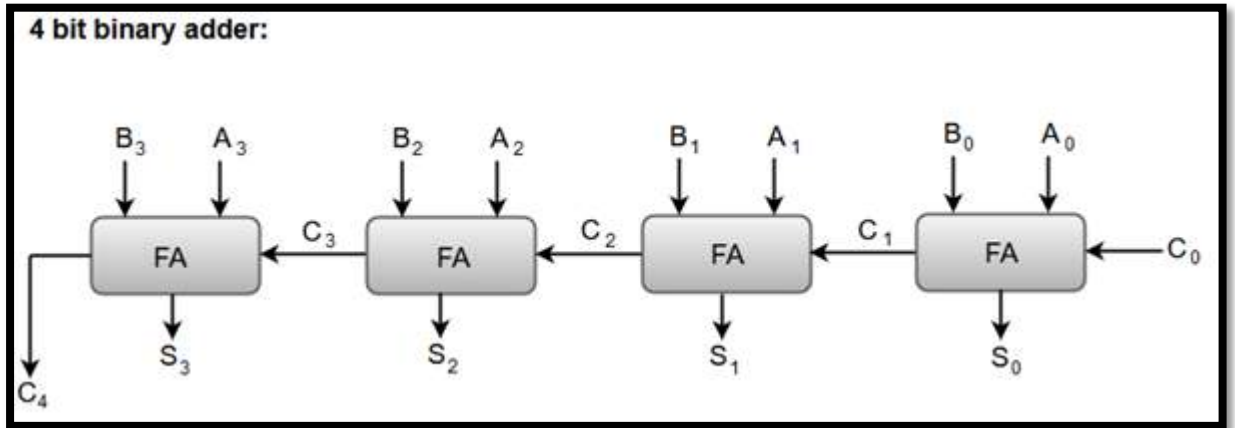


Fig. 1 a- Logic diagram of the full-adder, b- block diagram of full- adder

1-3 The Binary Adder



$$\begin{array}{r}
 C_3 \ C_2 \ C_1 \\
 A_3 \ A_2 \ A_1 \ A_0 \\
 B_3 \ B_2 \ B_1 \ B_0 \\
 \hline
 C_4 \ S_3 \ S_2 \ S_1 \ S_0
 \end{array}$$

Ex1:

$$\begin{array}{r}
 111 \quad C \\
 0111 \quad A \\
 0101 \quad B \\
 \hline
 1100
 \end{array}$$

Ex2:

$$\begin{array}{r}
 \quad \quad C \\
 1000 \quad A \\
 1000 \quad B \\
 \hline
 10000
 \end{array}$$

2- Binary Subtraction

- 0-0=0
- 1-1=0
- 1-0=1
- $10_2 - 1 = 1$

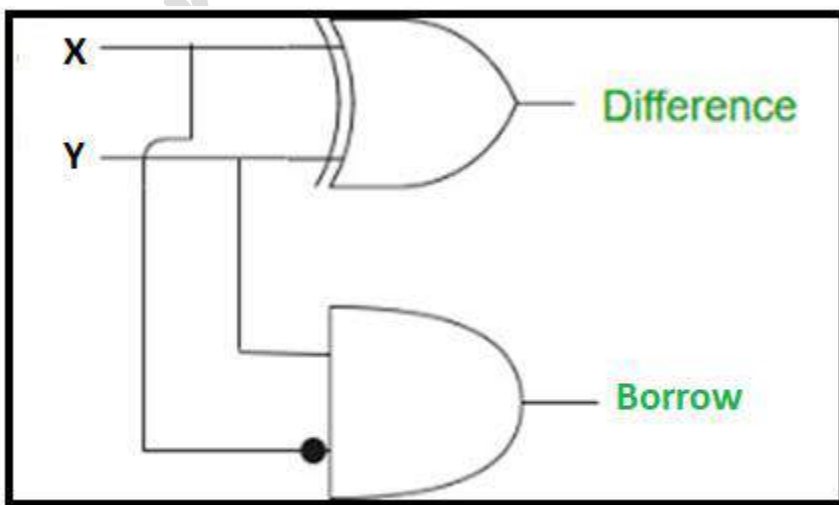
- When we have 0-1 we have to borrow from the next higher column so 10_2 is created and the last of the four rules is applied (exactly as decimal)

Ex.

$$\begin{array}{r}
 11 \\
 -01 \\
 \hline
 10
 \end{array}
 \qquad
 \begin{array}{r}
 11 \\
 -10 \\
 \hline
 01
 \end{array}
 \qquad
 \begin{array}{r}
 010 \\
 \cancel{1}01 \\
 -011 \\
 \hline
 010
 \end{array}
 \qquad
 \begin{array}{r}
 0110 \\
 \cancel{1}001 \\
 -0110 \\
 \hline
 0011
 \end{array}$$

2-1 Half – Subtractor

It performs the subtraction of two binary numbers. Hence it has 2-inputs and 2-outputs (D and B). B for borrow, gives the binary signal that informs the next stage that a 1's has been borrowed.



Inputs		Outputs	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$X > Y$ $0-0=0$

$1-0=0$

$1-1=0$

$X < Y$ $0-1=$ you need to borrow from the next stage

010

$$\begin{array}{r} 101 \\ - 011 \\ \hline 010 \end{array}$$

2-2 Full-Subtractor

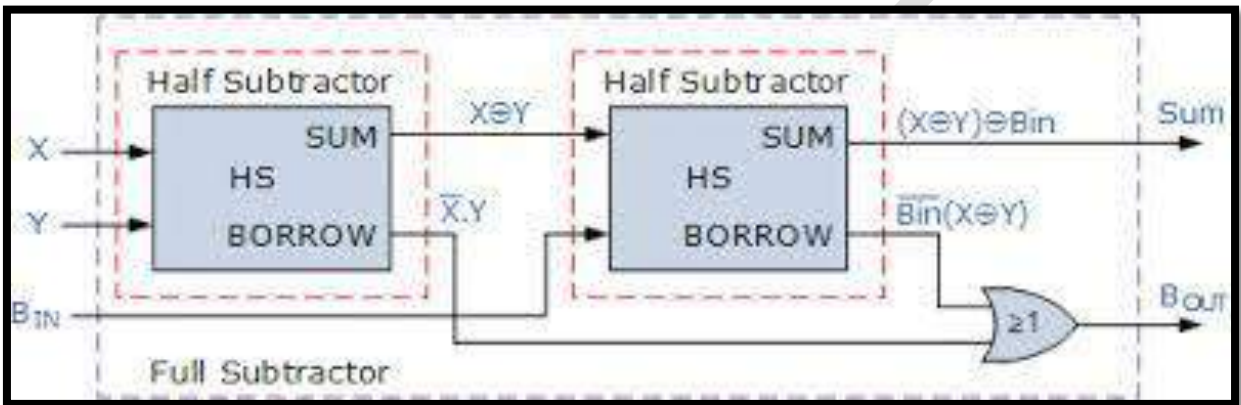
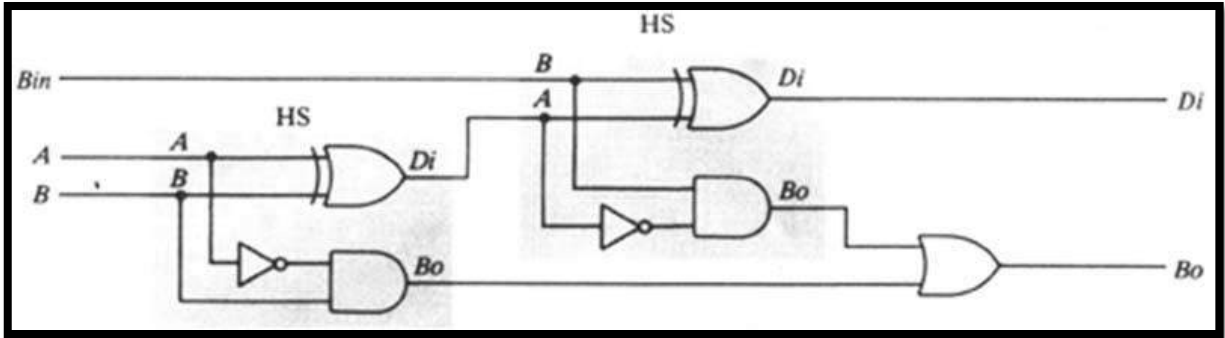
The full subtractor is a combinational circuit which has three inputs and two outputs. It performs subtraction in two bits taking account that a 1 may have been borrowed by a lower significant stage.

Inputs			Outputs	
X	Y	Z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = X \oplus Y \oplus C$$

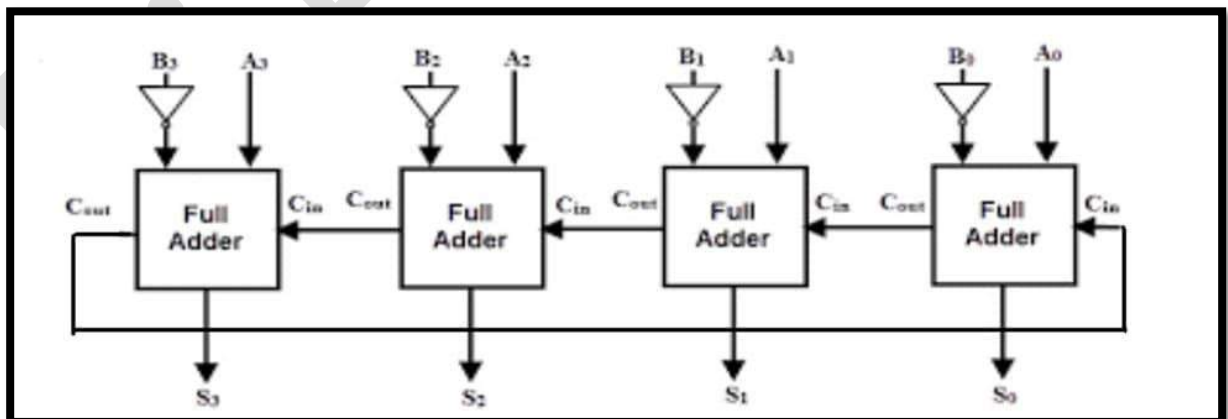
$$B = \bar{Y}Z + \bar{X}Z + \bar{X}Y$$

Lecture 5



1ST Complement Subtractor

- Invert each 1 to 0 and each 0 to 1. Exp. 0011 , 1st complement is 1100, 1001 , 1st complement is 0110
- When there is endround carry. The answer is positive.
- When there is no endround carry. The answer is negative and then recomplementary the results



Lecture 5

Exp: using 1st complementary method subtracte 111_2 from 101_2 , 01101_2 from 11011_2

$$\begin{array}{r}
 111 \\
 - 101 \\
 \hline
 111 \\
 + 010 \text{ (1}^{\text{st}} \text{ complement)} \\
 \hline
 1001 \\
 \xrightarrow{1+} \\
 \hline
 010 \text{ (+) endround}
 \end{array}$$

$$\begin{array}{r}
 01101 \\
 -11011 \\
 \hline
 01101 \\
 +00100 \\
 \hline
 10001 \text{ (-) no carry then} \\
 \text{recomplementary the results} \quad \boxed{-01110}
 \end{array}$$

Exp: using 1st complementary method subtracte, 11011_2 from 01101_2
 $11011 = 1^{\text{st}} \text{ complement } 00100$

$$\begin{array}{r}
 11 \\
 01101 \\
 +00100 \\
 \hline
 10001 \text{ then recomplementary the results} \quad \boxed{-01110}
 \end{array}$$

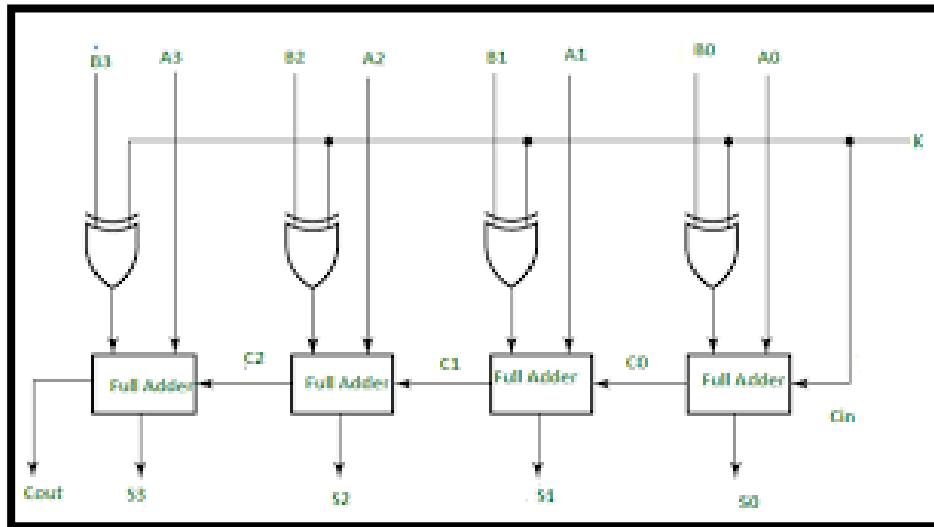
2nd Complement Adder/Subtractor

To get 2's complement of binary number is 1's complement of given number plus 1 to the least significant bit. For example 2's complement of binary number 10010 is $(01101) + 1 = 01110$.

$$S = A + \hat{B}$$

- When there is no last carry, the answer (-ve) and in the 2nd complement of the actual magnitude.

Lecture 5

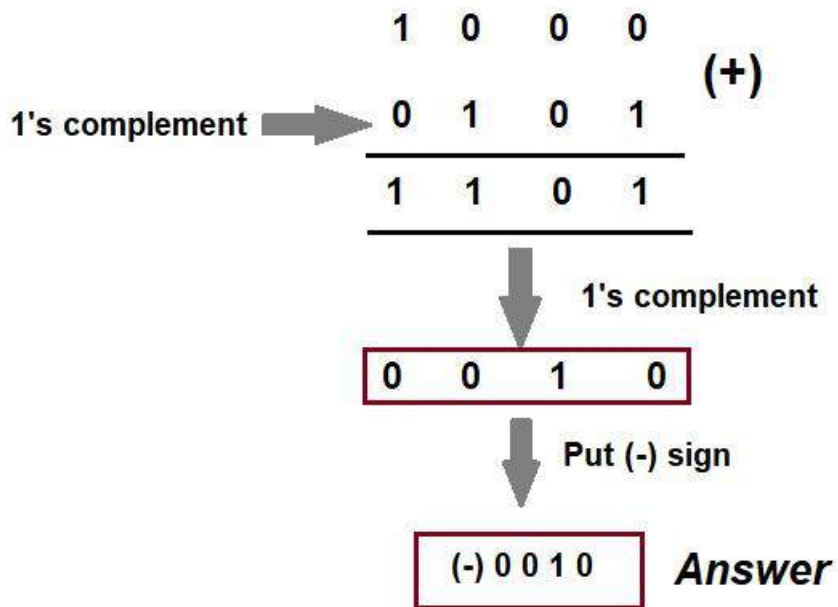
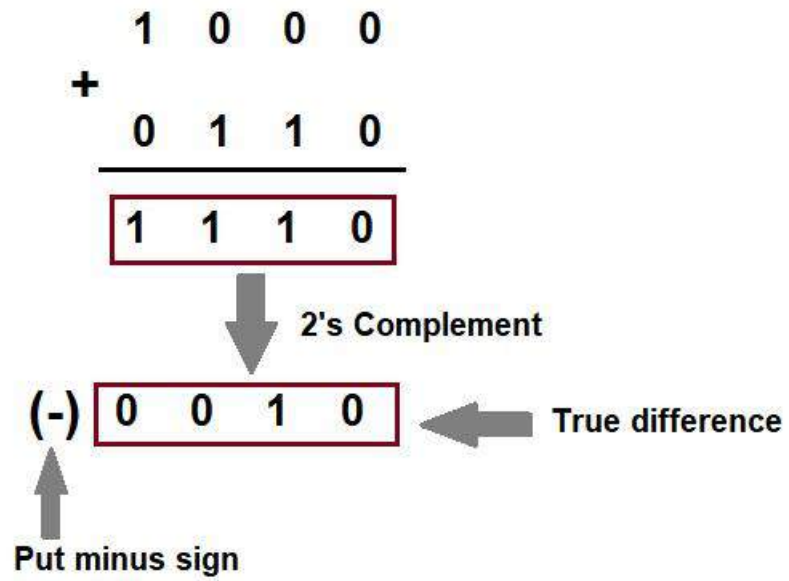


- SUB B bits through the XOR-gates= controlled inverter
- When SUB is low then B-bits pass through the controlled inverter to the full adders. The circuit produce the SUM of A+B.
- When SUB is high, then the B-bits are inverted before reaching the full adders.

$$\begin{array}{r}
 1111 \\
 + 0101 \text{ 1's complements} \\
 \hline
 \text{Carry } 10100 \\
 \phantom{\text{Carry}} 1 \text{ Add} \\
 \hline
 0101
 \end{array}$$

$$\begin{array}{r}
 1111 \\
 + \\
 0101 \\
 \hline
 \text{Carry } \textcircled{1} 0100 \\
 \phantom{\text{Carry}} + 1 \\
 \hline
 \boxed{0101} \text{ Answer}
 \end{array}$$

Lecture 5



Chapter Five: Memory elements: Flip-Flops

Till now we concern with combinational logic circuits which are composed of a number of different logic gates. The output is based on the input variables. The output is either expressed by a Boolean equation or truth table or both.

A **Sequential circuit** combinational logic circuit that consists of inputs variable (X), logic gates (Computational circuit), and output variable (Z).



Figure: Combinational Circuits

Combinational circuit produces an output based on input variable only, but **Sequential circuit** produces an output based on **current input and previous input variables**. That means sequential circuits include memory elements which are capable of storing binary information. That binary information defines the state of the sequential circuit at that time. A latch capable of storing one bit of information.

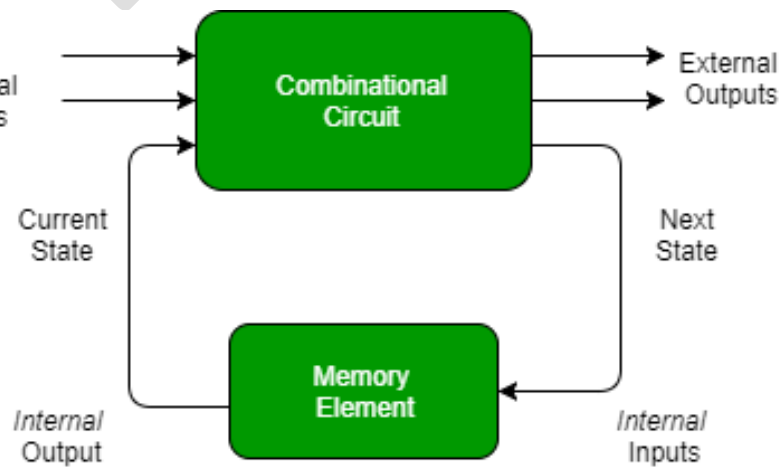


Figure: Sequential Circuit

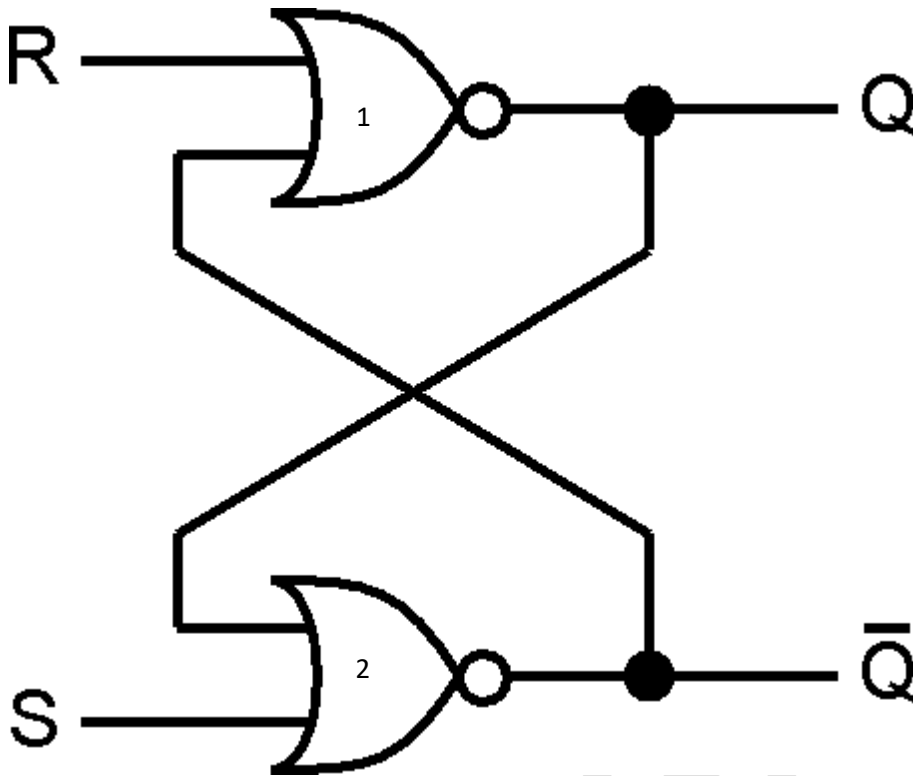
Types of Sequential Circuits – There are two types of sequential circuit:

1. Asynchronous sequential circuit – this circuit do not use a clock signal but uses the pulses of the inputs. These circuits are faster than synchronous sequential circuits because there is no clock pulse and change their state immediately when there is a change in the input signal.
2. Synchronous sequential circuit – this circuit uses clock signal and level inputs (or pulsed). The output pulse is the same duration as the clock pulse for the clocked sequential circuits. Since they wait for the next clock pulse to arrive to perform the next operation, so these circuits are bit slower compared to asynchronous. Level output changes state at the start of an input pulse and remains in that until the next input or clock pulse.

Flip-flops circuits can maintain a binary state indefinitely until directed by an input signal to switch states. The major differences between flip-flops types are based on the number of inputs and the manner in which the inputs affected the binary states.

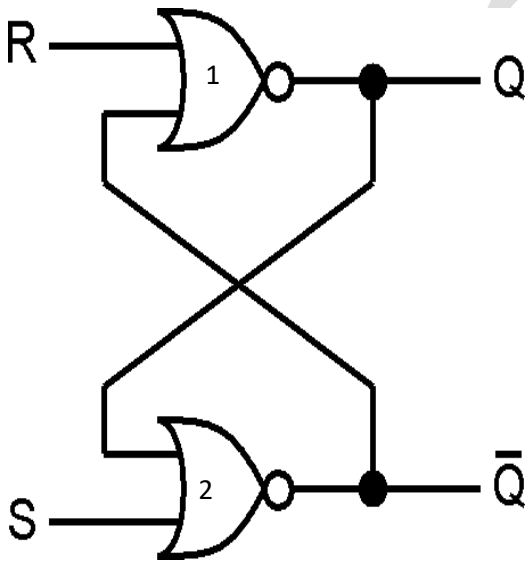
1- RS Flip-flop

- It is simplest storage devices called reset-set (RS) flip-flop which can be constructed by using two NAND or two NOR gate. It has two inputs, one is called “**SET**” which will set the device (output =1) and is labelled S and another is known as “**RESET**” which will reset the device (output = 0) labelled as R. The RS stands for **SET/RESET**. In our study we will take NOR gate as RS flip flop.



Input		Output
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

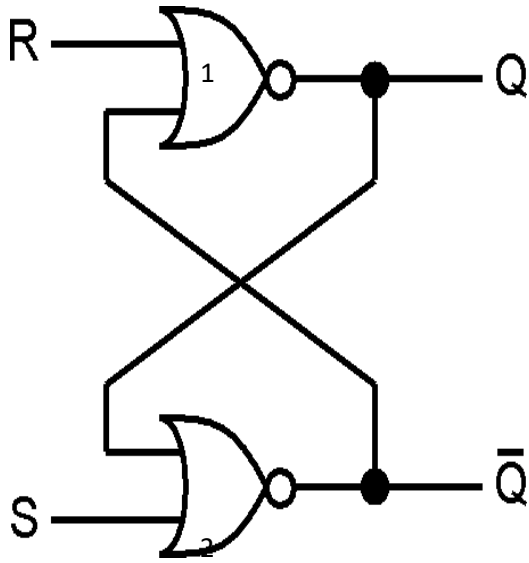
1- S=0, R=1 (reset)



- R is equal to 1, Q becomes 0, The inputs to NOR-2 are (0,0), so its output will change to 1, $\bar{Q}=1$. So now we have the binary digit 0 at Q. This means the logic level 0 is stored at Q and logic level 1 is stored at \bar{Q} .

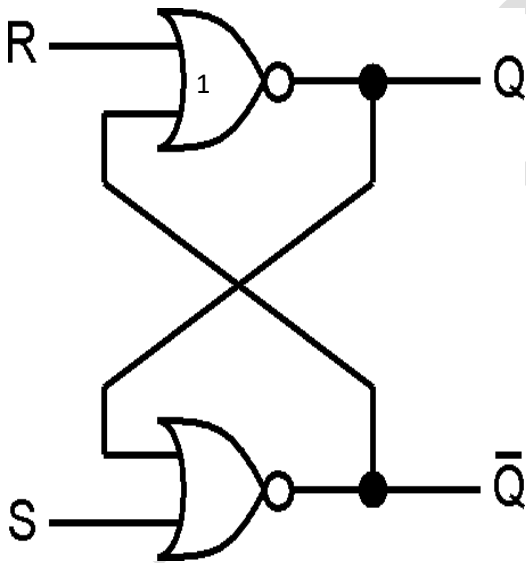
- The data is stored even if the inputs removed. Let us put R=0, and S stay =0, $\bar{Q}=1$ and R=0 depending on the truth table Q=0. i.e. the data stored (memory condition).

2- S=1, R=0 (set)



Here we also depend on the truth table, when $S=1 \bar{Q}=0$, which feedback to NOR 1 so $R=0$, $\bar{Q}=0$ then $Q=1$. Again if we removed the inputs ($R \ \& \ S=0$) Q is still equal to 1 and according to the truth table $0 \ 1=0$ so $\bar{Q}=0$. It's a memory state. So RS flip-flop is an asynchronous device.

3- R=1, S=1 (NOT USED)

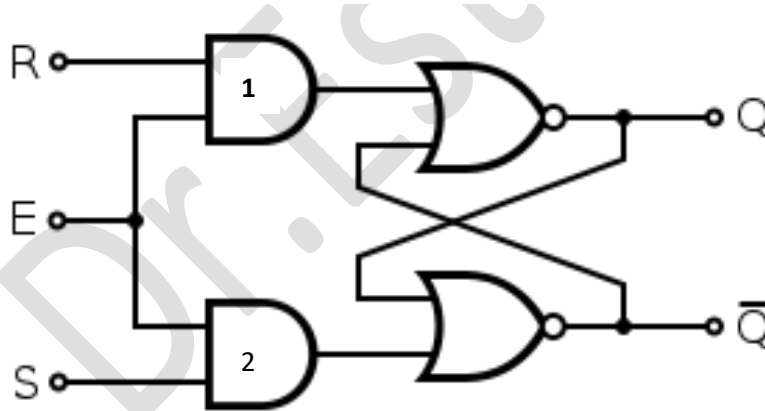
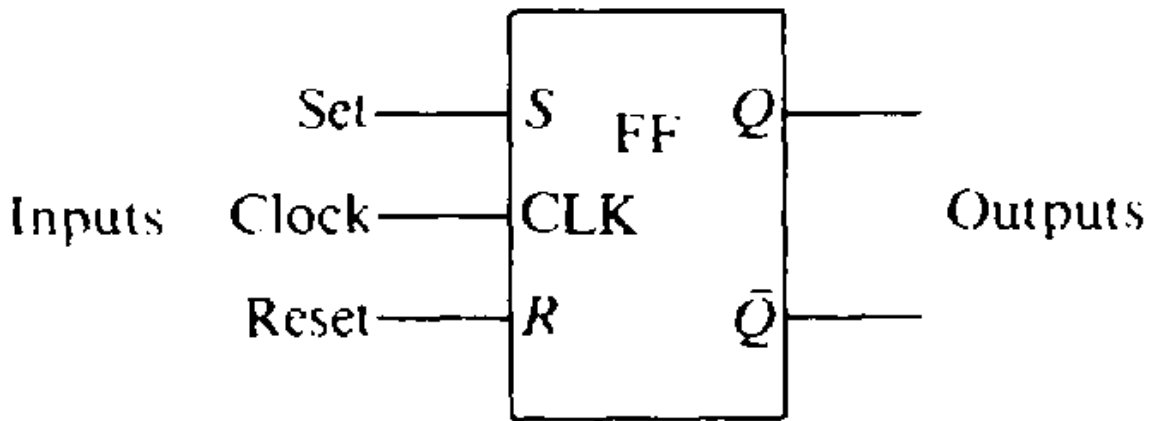
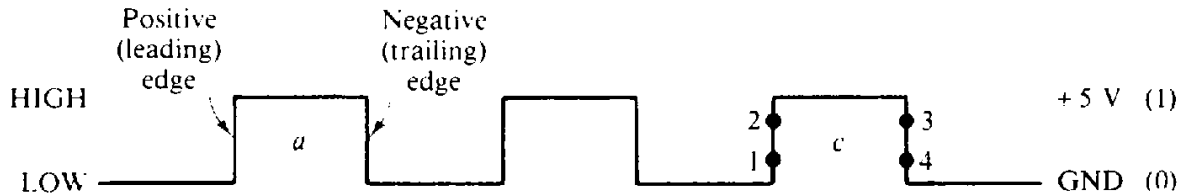


In this case $Q=0 \ \& \ \bar{Q}=0$, i.e. $Q=\bar{Q}=0$, which can't be since \bar{Q} is the complement of Q . but if we make $S=0, R=0$ starting from $Q=0, \bar{Q}=1$ and that is not stored data . now if we started from $\bar{Q}=0, Q=1$

S	R	Q	\bar{Q}
0	0	Memory (as before)	
0	1	0	1
1	0	1	0
1	1	NOT USED	

2- CLOCKED RS Flip-flop

The clocked RS flip-flop adds a valuable synchronous feature to the RS latch. The clocked RS operates in steps with the clock or timing devices [it operates synchronously]. The output won't work randomly



-Clocked RS Flip-Flops is the addition of two AND gates at the R and S inputs and the CLOCK (C) to control whether a flip-flop can be enabled or disabled.

Lecture 6

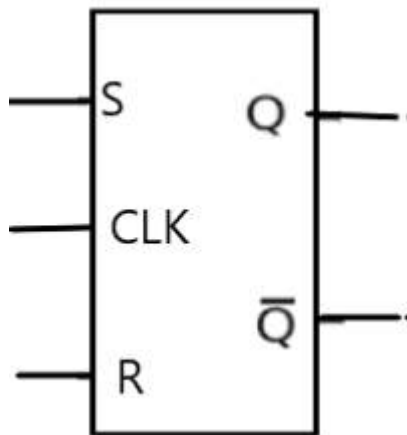
- When $CLK=0$: no matter what the logic level of R or S are, the output of the AND-Gates will be 0. The inputs of the flip-flop are (0, R=0, S=0), so there will be no change of the state of the flip-flop i.e. the flip flop store its value.

- When $CLK=1$: with $S=1$, AND-Gate 2 is enabled and its output will be 1. The S signal has gone through the AND-Gate to SET the flip-flop. $R=0$, AND-Gate 1 will be disabled and $R=0$ will be at the input of the flip-flop.

The same happens for the rest of the truth table.

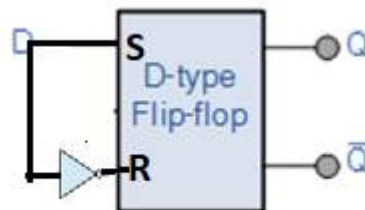
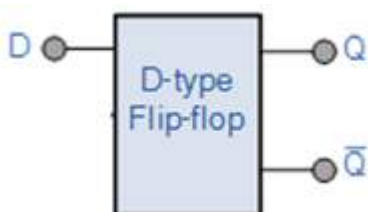
- In summary, when $CLK=1$ the S and R has their effect on the flip-flop.

This is the idea of synchronizing; the flip-flop can change its state only when the $CLK=1$. The appropriate timing of the CLK is chosen according to the time we want to retain (store) a certain state of the flip-flop.



3- D flip-flop

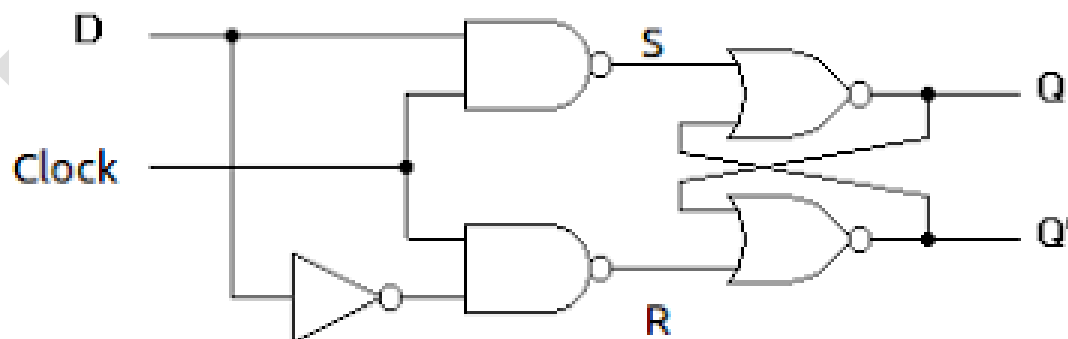
- From RS flip flop we saw that S and R are complement to each other ($S=0, R=1$ and $S=1, R=0$). So instead using two inputs we can use only one input and use inverter (NOT gate) to have second input.



- The effect is that D input condition is only copied to the output Q when the clock input is active.
- When $D=0$: $S=0$, $R=1$ the flip-flop will RESET $Q=0$
- When $D=1$: $S=1$, $R=0$ the flip-flop will SET $\bar{Q}=1$
- This can be seen in the truth table.
- It can be seen that $Q=D$

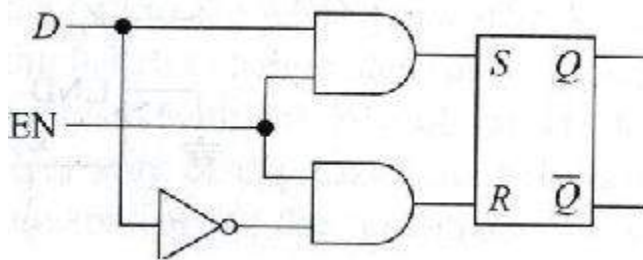
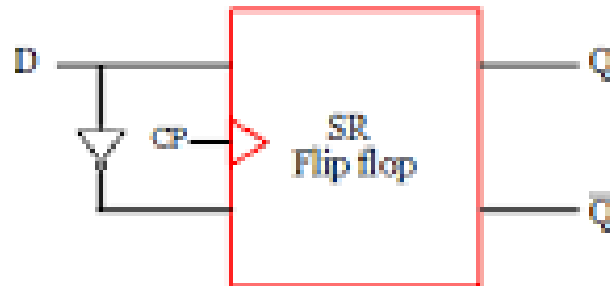
Clocked D flip-flop

- The D flip-flop has only a single **data** input (D) and a clock input (CLK).
- Why we use CLK? To avoid an additional inputs “ If If this data input is held HIGH the flip flop would be “SET” and when it is LOW the flip flop would change and become “RESET”. However, this would be rather pointless since the output of the flip flop would always change on every pulse applied to this data input”.
- As it can be seen that the truth table is valid when $CLK=1$. When $CLK=0$ both AND-Gates are disabled and D is prevented from the flip-flop.



Lecture 6

- In this case only when $CLK=1$, $D=Q$ and the input signal will transfer to the output.

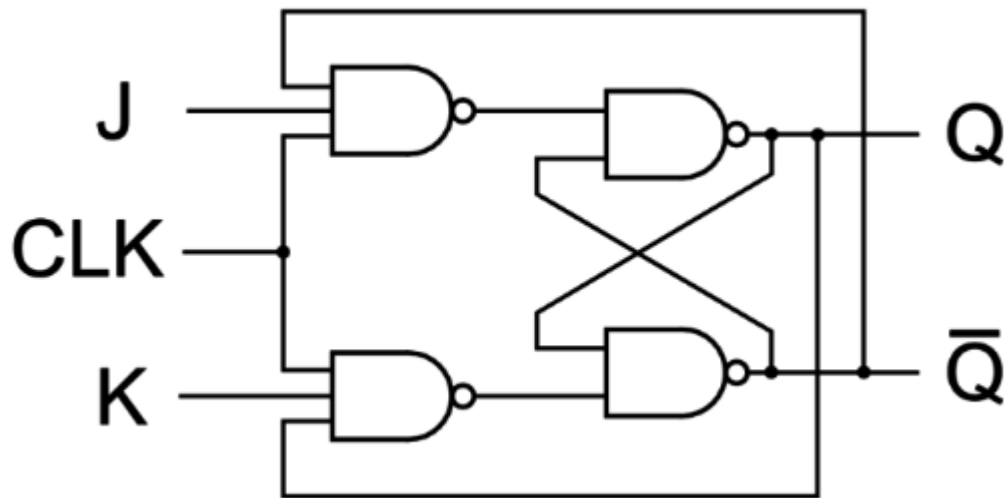


D	CLK	$Q(t+1)$	Comments
1	↑	1	Set
0	↑	0	Reset

↑ = clock transition LOW to HIGH

1- J-K Flip-Flop

- A gated S R flip flop with the addition of a clock input circuitry is basically the J k flip flop.
- This circuit prevents the invalid output condition which occurs when both inputs are high. The new addition here gives us four possible outputs of the flip flop. The output may be – No Change, Logic 0, Logic 1 & Toggle.



Clk	J	K	Q
0	X	X	Memory
1	0	0	Memory
1	0	1	0
1	1	0	1
1	1	1	Toggle (\bar{Q})

Lecture 7

1- CLK=0, Memory

2- CLK=1, J and K =0 (Memory)

Here $J=K=0$ both AND gates are disabled and there is no effect of the CLK pulse and the output remains what it was before the arrival of the pulse.

3- J=0, K=1 (RESET)

When $J=0$, $K=1$, and input gave is 0 then the output at point Q is $\bar{Q}=0$

4- J=1, K=0 (SET)

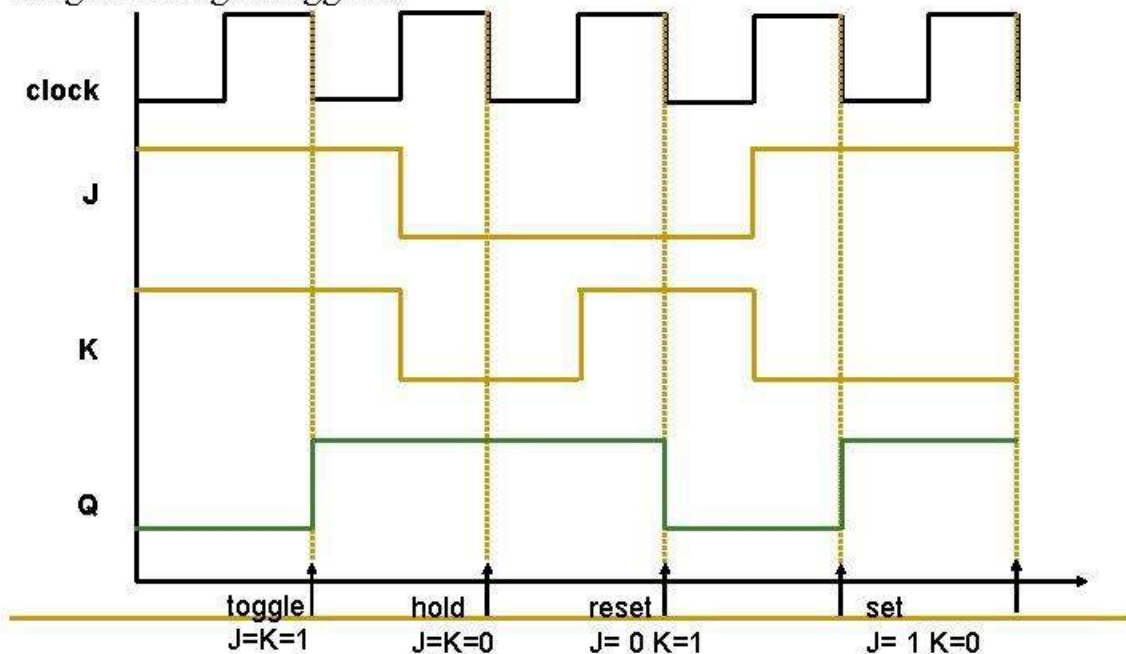
When $J=1$, $K=0$, and input gave is 0 then the output at point Q is $\bar{Q}=1$

5- J and k =1 (HIGH)

It's a problem. If we take $Q=0$, $\bar{Q} = 1$. And when $Q=1$, the output value \bar{Q} will 0. We see that the value of the Q and \bar{Q} will complement each other means system is not an invalid state or not in a running state.

Timing diagram for JK Flip-flop

Negative Edge Triggered



Lecture 7

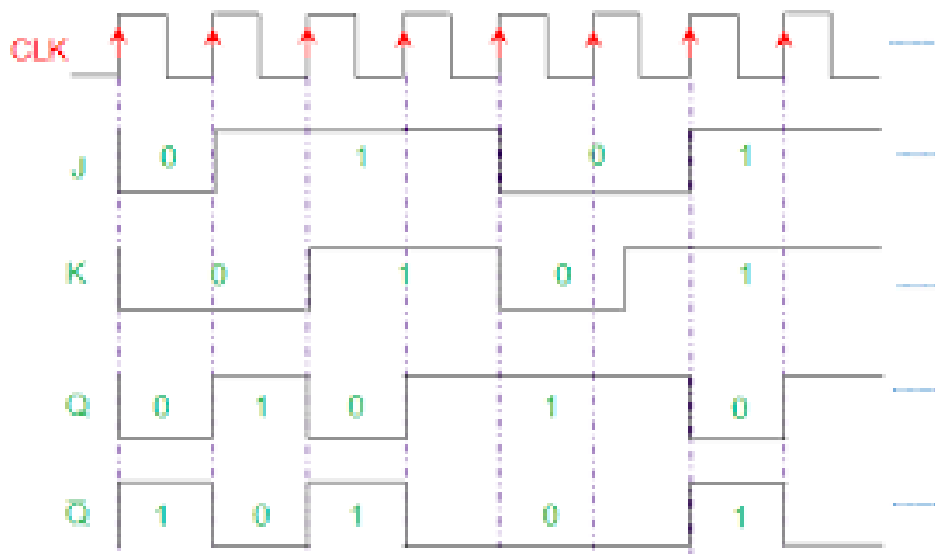
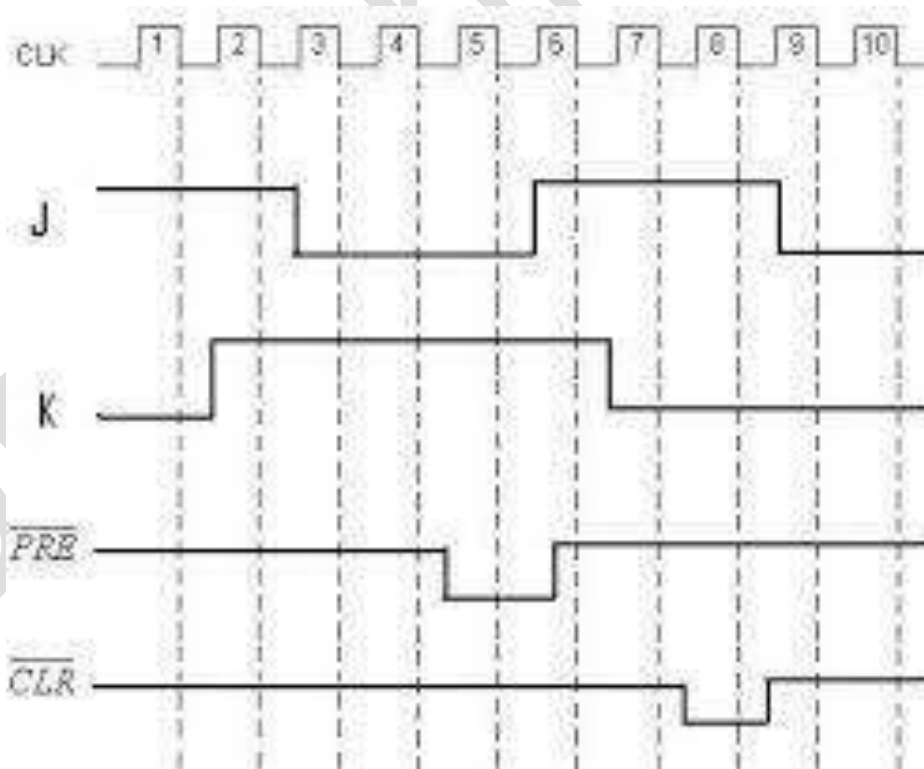


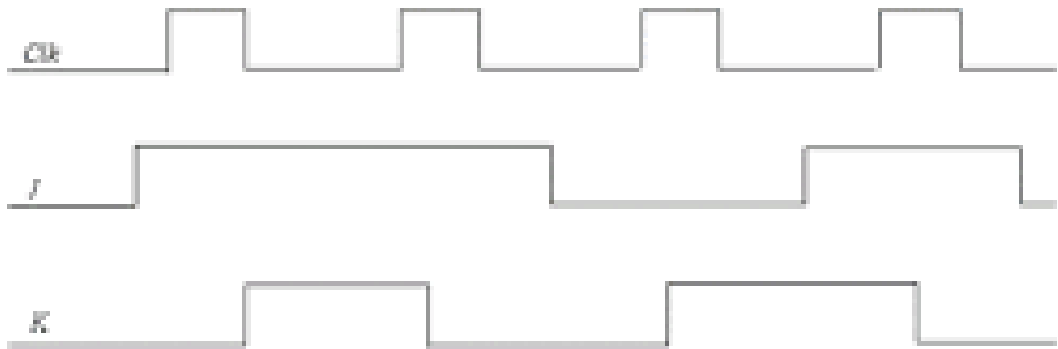
Figure 3 Timing diagram for positive edge-triggered JK flip-flop



Lecture 7

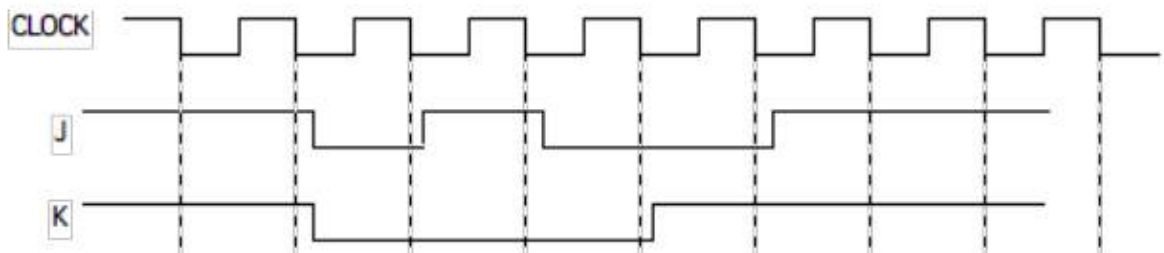
PROBLEM 3 (points: 5)

- a. Derive the output waveforms of a JK flip-flop for the input waveforms depicted in the following figure



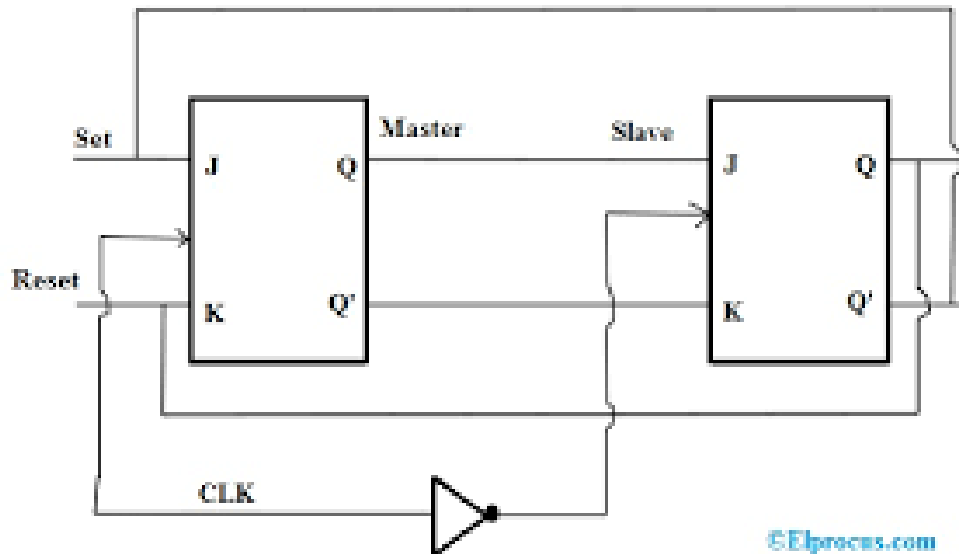
- b. Design a binary up-counter that counts in the sequence 0, 1, 2, 3, 4, 5, 0, ... which is a modulo-6 counter by D, JK, and T flip-flops.

The following waveform specifies the inputs of a negative-edge triggered JK flip-flop. Assuming that the output Q of the flip-flop is initially undefined, add the timing diagram of Q to the waveform.



2- Master-Slave Flip-flop

- A master-slave flip flop is constructed from two separate flip-flops. One circuit services as a master and the other serves as a slave.
- The mater-slave JK flip-flops can constructed by using NAND gates



- As we can see, it consist two JK flip-flop one is called master and the other is called slave.

Working of a master slave flip flop

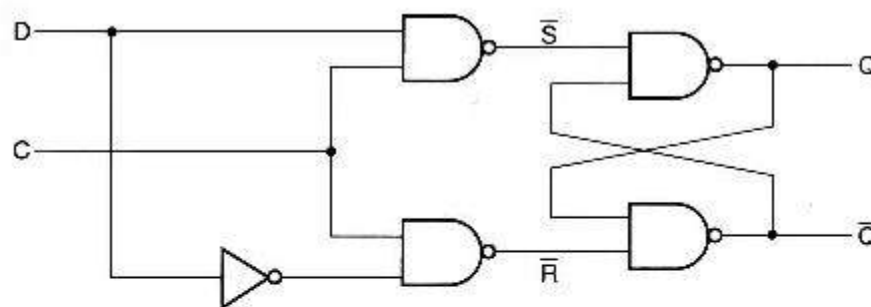
- 1- When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained.
- 2- Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave.
- 3- If $J=0$ and $K=1$, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master.

Lecture 7

- 4- If $J=1$ and $K=0$, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master.
- 5- $J=1$ and $K=1$, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.
- 6- If $J=0$ and $K=0$, the flip flop is disabled and Q remains unchanged.

3- Preset and Clear

Asynchronous inputs on a **flip-flop** have control over the outputs (Q and not- Q) regardless of clock input status. These inputs are called the **preset** (PRE) and **clear** (CLR). The **preset** input drives the **flip-flop** to a set state while the **clear** input drives it to a **reset** state.



(a) Logic diagram

C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

(b) Function table

Field Effect Transistor

Field Effect Transistor (FET) is a unipolar device and its operation depends on only one type of charge carriers either holes or free electrons, thus FET has majority carriers not minority carriers. While BJT has two types of charge carriers, i.e. holes and free electrons and thus we call it a bipolar device.

The Field Effect Transistor, FET, is a three terminal active device that uses an electric field to control the current flow and it has high input impedance which is useful in many circuits. It is a key electronic component using within many areas of the electronics industry.

A FET is a voltage-controlled semiconductor device. Its advantages over bipolar junction transistors are:

- 1- FET is a unipolar device. Transistor is bipolar.
- 2- FET is a voltage controlled device. Transistor is a current controlled device.
- 3- FET has very high input resistance. Transistor has low input resistance.
- 4- FET has small voltage gain. Transistor has higher voltage gain than the FET.
- 5- The gate in the FET is reverse biased. The base in the transistor is forward biased.

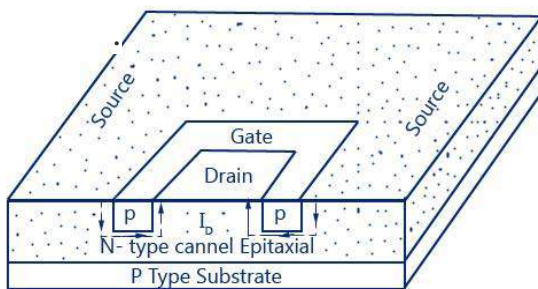


There are two types of FET: Junction FET (JFET) and metal oxide semiconductors (MOSFET) or insulated gate FET.

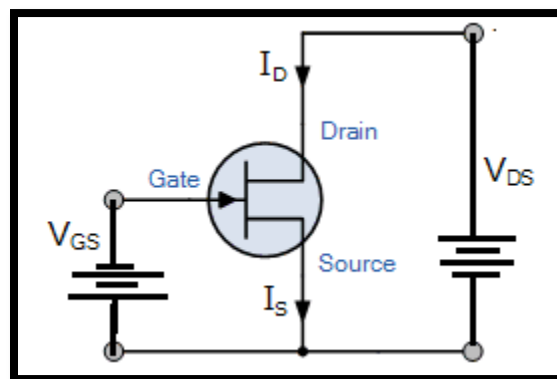
1- Junction Field Effect Transistor (JFET)

a) Structure

A JFET has a base semiconductor known as channel; it can be N or P-type. A voltage supply across the ends of the channel causes the flow of current. The two ends of the channel are known as source and drain. If the channel is N-type the current is due to the electrons, while if the channel is P-type the current is due to holes. The majority carriers enter the channel from source (S) and source current is denoted as I_S . The current entering the drain is denoted by I_D . The drain is positive with respect to the source (drain to source voltage V_{DS}). If the channel is N-type materials, two heavily doped p-type regions are found on opposite sides of the channel. Each of these p-regions is called a gate; they are connected together and appear with only one terminal. There is no current in the gate because of the reverse biasing on the gate –source junction. There is a junction between the gate and the channel so there exists a depletion layer on both sides of the junction in the channel and in the gate. The depletion layer on the gate side is of no importance but the depletion layer in the channel side is of importance in the operation of the JFET. Since the gate is on both sides of the channel the depletion layers on both sides of the channel will reduce the width of the channel thus reducing the current from the source to the drain.

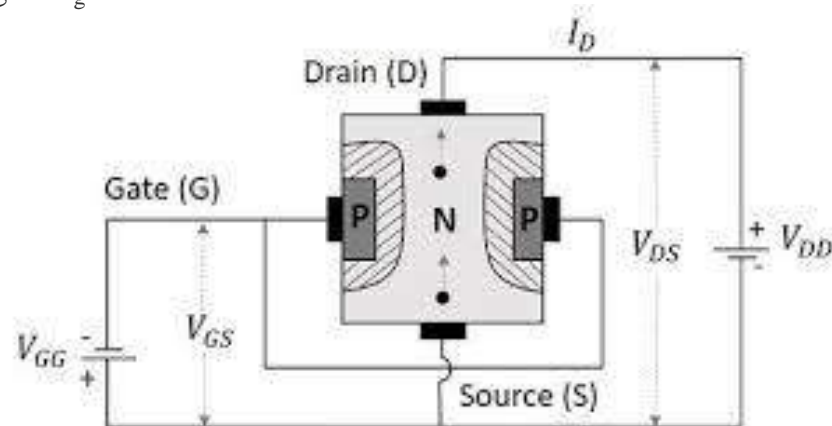


Geometry of JFET

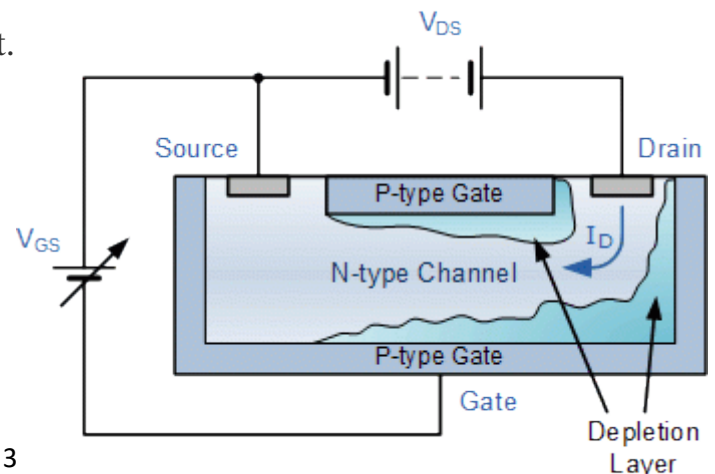


Operation

- ❖ Figure below shows the normal polarities for biasing an N-channel JFET. The idea is to apply a negative voltage between the gate and the source. Since the gate is reversed-biased, only a very small reverse current flows in the gate $I_g=0$.



- ❖ The name field effect is related to the depletion layers around each PN junction. Free electrons moving between the source and the drain must flow through the narrow channel between depletion layers. The size of these depletion layers determines the width of the conductive channel. The more negative the gate voltage the narrower the conductive channel becomes, i.e. the conductivity is reduced, because the depletion layers get closer to each other. Therefore, the gate voltage controls the current that flows between the source and drain. The more negative the gate voltage, the smaller the current.



b) Symbol and circuit configuration

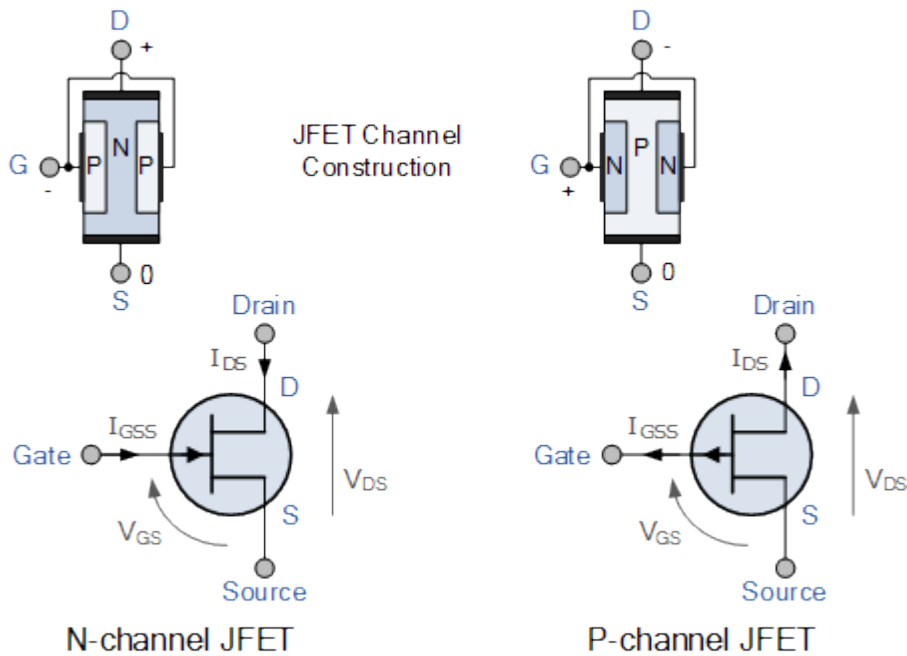


Fig. above shows the symbol and circuit for n- and p-channel JFET. For n-channel JFET, I_D and V_{DS} are positive and V_{GS} is negative.

c) JFET Characteristics

The curves plotted between the current value at the drain and the voltage applied in between drain and the source for different values of the gate-source voltage are the output characteristic curve that are also referred to as the **drain characteristics**.

The regions of the drain characteristics of the JFET are

1. **Ohmic Region:** When small values of V_{GS} the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor. It is also known as the linear region.

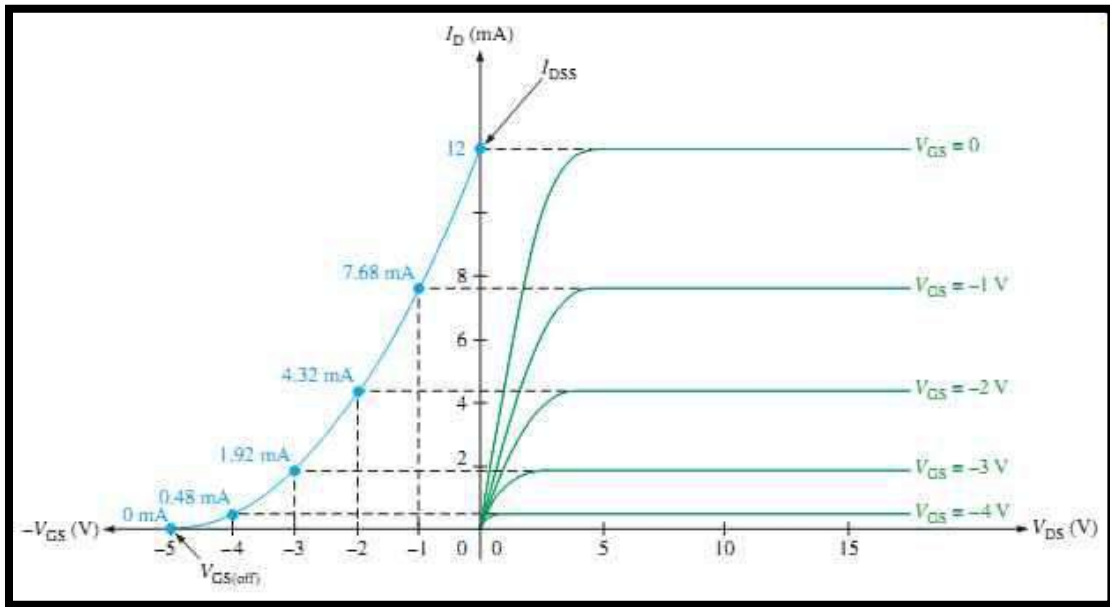
2. **Saturation or Active Region** – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.
3. **Breakdown Region** – The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current. But if the drain to source voltage is increased further then the device reaches the breakdown region in which the drain current increases indefinitely.

NOTES

- ❖ **Cut-off Region:** This is also known as the **pinch-off region** were the Gate voltage, V_{GS} is sufficiently negative so as to cause the channel to close making the drain current equal to zero. As the drain voltage is increased the channel tends to become narrower and narrower and current at the drain terminal gets smaller. At a particular drain to source voltage called the **pinch-off voltage** the drain current reaches the saturation level. [**Cut off region is due to V_{GS} but the pinch off voltage is due to V_{DS}**].
- ❖ **Pinch –off voltage V_p :** is the drain voltage above which the drain current become almost constant for shorted gate condition. When the drain voltage equals V_p , the conducting channel becomes extremely narrow and the depletion layers almost touch, further increase in drain voltage produce only the slightest increase in drain current.
- ❖ Now if a negative voltage is applied to the gate terminal then, in that case, the channel present at the gate reverse biases and the saturation current starts decreasing further. At a particular gate voltage the device stops conduction this is called the **cut-off-voltage**.

- ❖ **Shorted-gate condition-** if the gate voltage is reduced to zero, the gate is effectively shorted to the source. This is called the short-gate condition.
- ❖ I_{DSS} - it is the maximum drain current at shorted gate.

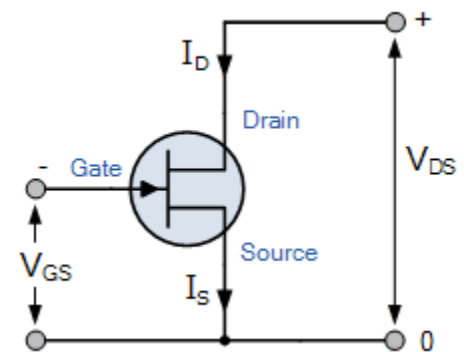
When $V_{GS} = V_{GS(off)}$ the depletion layers touch, cutting off the drain current. Since V_p is the drain voltage that pinches off current for the shorted-gate condition. $V_p = -V_{GS(off)}$



Tranconductance

$$I_d = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$|V_{GS(off)}| = V_P$$



Drain-Source Channel Resistance

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

$$g_m = -\frac{2I_{DSS}}{V_{GS(OFF)}} \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]$$

Where: g_m is the “transconductance gain” since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

d) JFET Biasing

1- Self-Bias

The idea is to use the voltage across the source resistor R_s to produce the gate-source reverse voltage.

From the above fig., since V_{GS} is reverse voltage negligible I_g flows through R_G . Therefore, the gate voltage with respect to ground is zero:

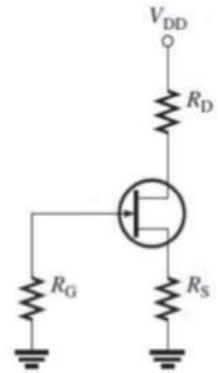
$$V_G = 0$$

The source voltage

$$V_s = I_d R_s$$

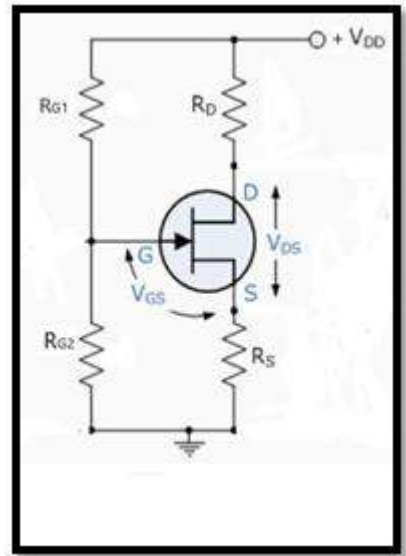
$$V_{GS} = V_G - V_s = -I_d R_s, \quad V_G = 0$$

R_s make a reverse bias between the gate and the source and maintain the value of I_d constant.

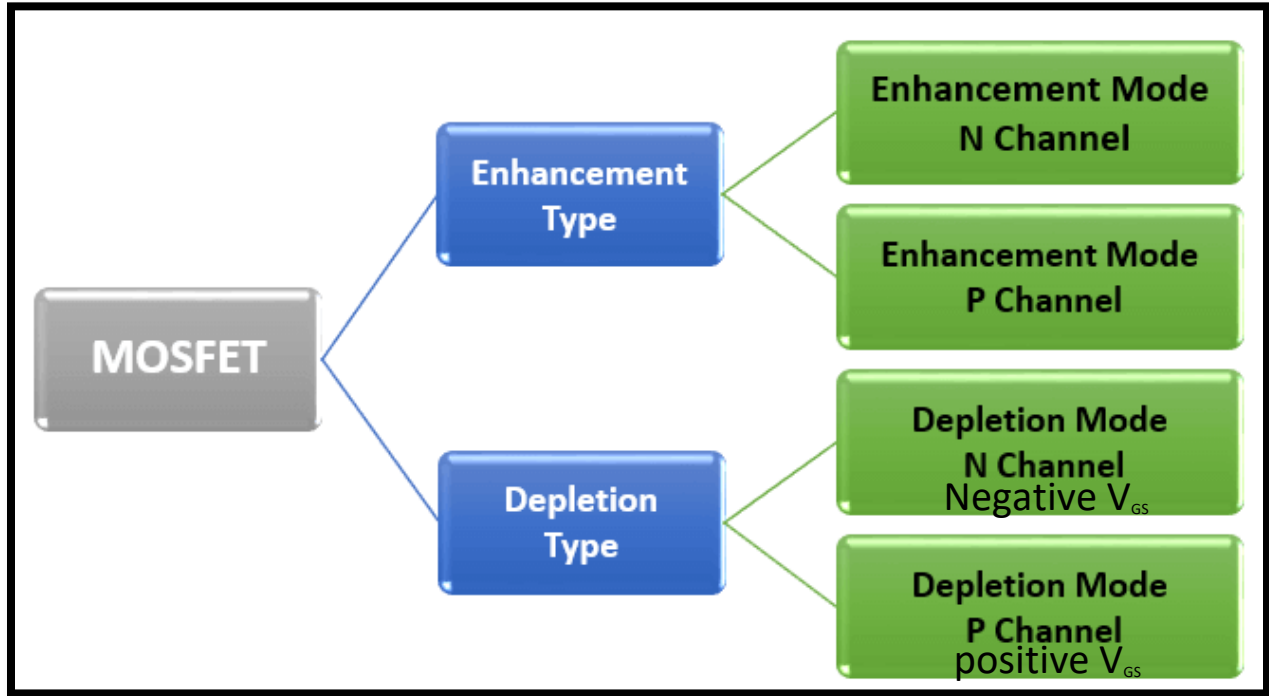


2- Voltage divider bias

$$V_{GS} = V_G - V_S \quad \text{for } V_{GS} \text{ to be negative } V_S > V_G$$

**2-Metal Oxide Semiconductor FET (MOSFET)**

The MOS (metal-oxide- semiconductor) transistor (or MOSFET) is the basic building block of most computer chips, as well as of chips that include analog and digital circuits. The **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a the gate is insulated (by a metal oxide layer) from the channel which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide.



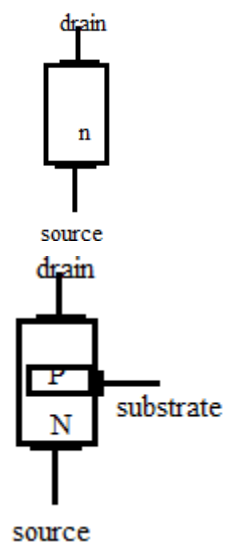
1- Depletion Type MOSFEET

Because the gate is insulated from the channel, one can apply negative or positive voltages to the gate,

a/ IGFET region

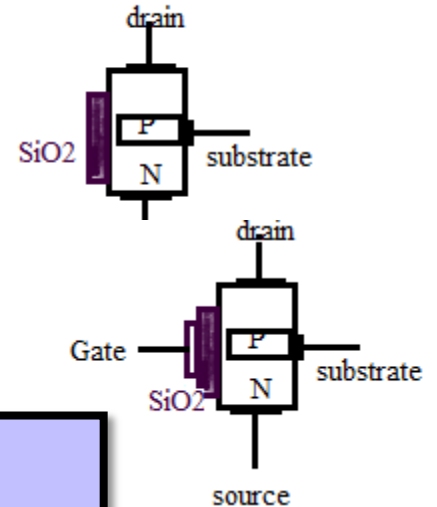
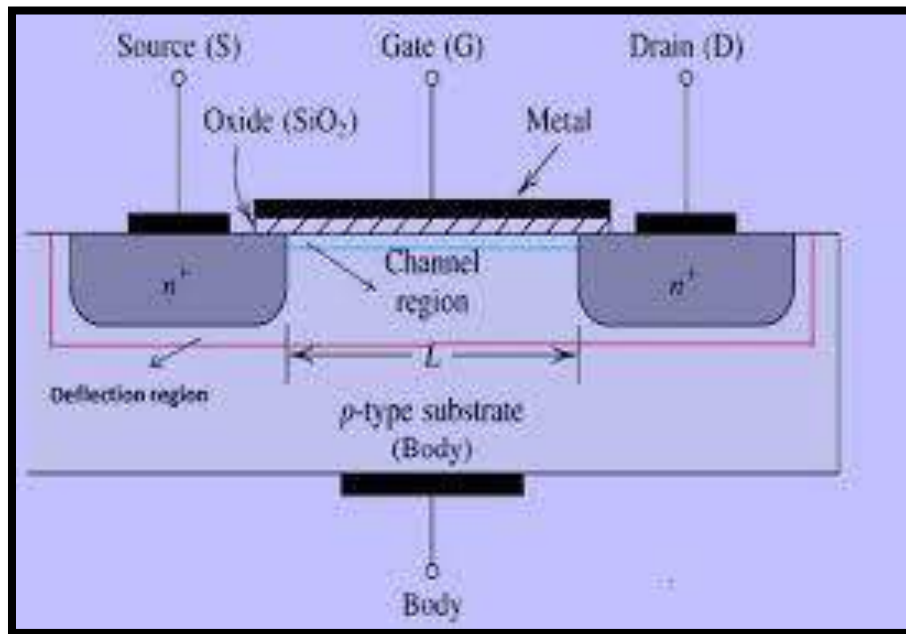
To begin with, there is an N-region with a source and drain as in fig.a, as (+ve) voltage applied to the drain-source terminals forces free electrons to flow from the source to the drain.

The MOSFET has a region called the substrate. This P-region reduces the channel between the source and the drain so that only a small passage remains at the left side in fig.b. Free electrons flowing from the source to the drain must pass through thin narrow channel (lightly doped).



A thin layer of silicon dioxide (SiO_2), an insulator, is deposited over the left side, fig.c, of the channel.

Finally, a metallic gate is deposited on the insulator; Fig. d. because of the gate is insulated from the channel a MOSFET is also known as IGFET.



The depletion type MOSEFET can be operated in two modes:

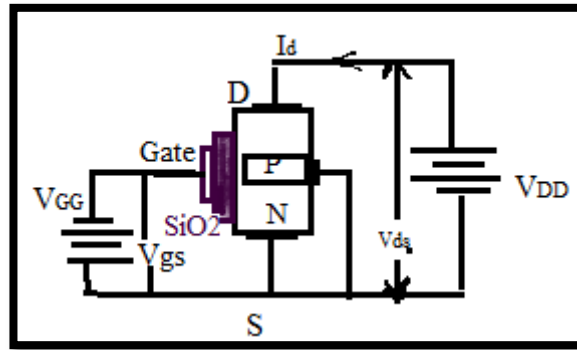
The depletion mode and the enhancement mode.

1- Depletion Mode:

This happens when negative voltage is applied on the gate .the operation here is similar to that of the JFET.

When V_{GS} is negative voltage, it depletes the N-channel of its electrons by inducting (+Ve) charge in it as shown in fig. a. The greater the negative voltage on the gate, the greater is the reduction in the number of electrons in the channel, and, consequently, the smaller it's the conductivity of the channel. So

the more (-Ve) gate voltage is, the smaller the current through the channel. Enough negative voltage on the gate ($V_{GS(off)}$) cuts off the current between the source and the drain. Therefore, with (-Ve) gate voltage the action of a MOSFET is similar to that of a JFET.



2) Enhancement mode

In this mode the gate is made positive with respect to the source. The input gate capacitor is able to create free electrons in the channel which increasing I_d . this positive voltage will attracts the electrons into the channel opposite to the gate thus increasing the conductivity of the channel. A increasing the positive voltage on the gate, increases the conductivity of the channel thus increasing the drain current

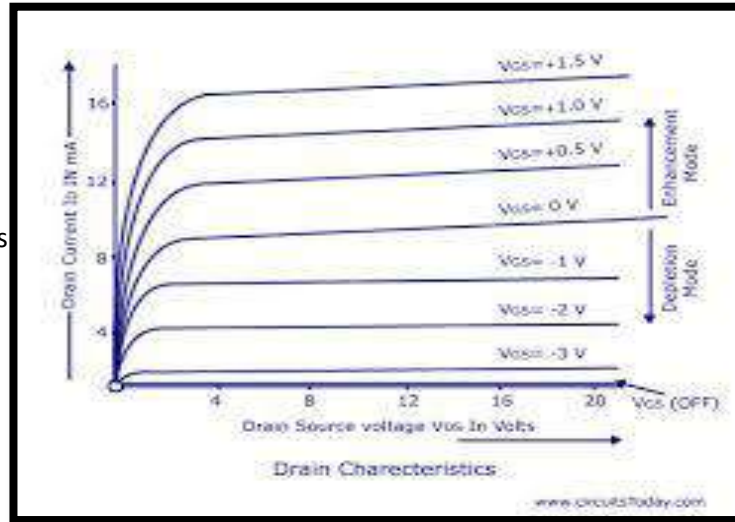
MOSFET Characteristics

This fig. shows typical drain curves for an N-channel D-MOSFET. For V_{GS} less than zero, we get depletion-mode operation, on the other hand, V_{GS} greater than zero given enhancement-mode of operation.

$V_{GS} < 0$ depletion

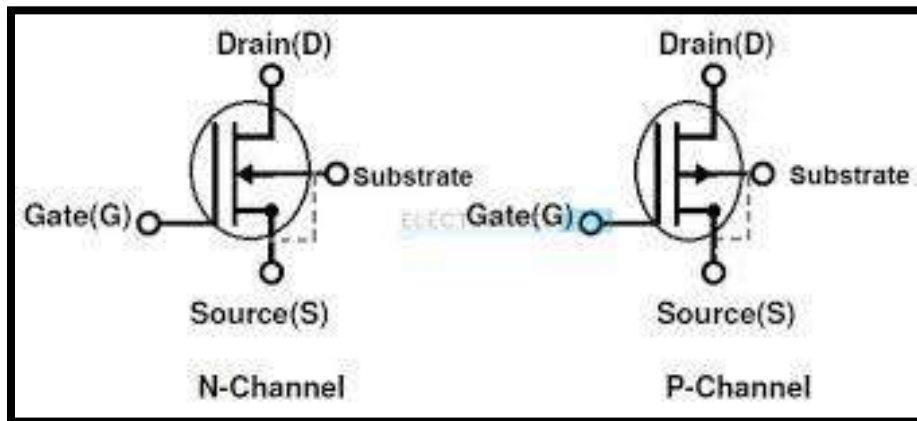
$V_{GS} > 0$ enhancement

Fig.a
Output characteristics



The transconductance curve, fig.b, I_{DD5} is no longer is the maximum possible current. As you can see, the transconductance curve extends to the right, so that I_d is greater than I_{DD5} in the enhancement mode. MOSFETs with a transconductance curve just like this fig. are easy to use since it does not require bias voltage. Q-value can be indicate by the vertical intercept where $I_d = I_{DD5} + V_{GS} = 0$. This means we do not have to provide any gate voltage at all, which simplifies biasing circuit.

Schematic Symbol



Biasing

D-MOSFET

1. The zero bias circuit.

$$V_{GS} = 0$$

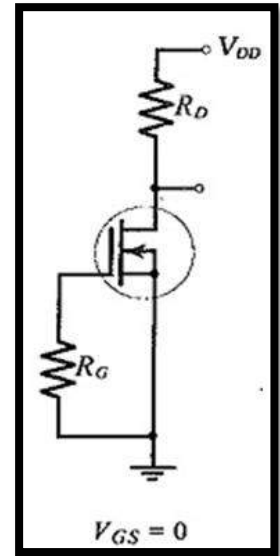
Being able to use zero V_{GS} is an advantage when it comes to biasing. It permits the unique biasing circuit in fig. b.

this simple circuit has no applied gate or source voltage.

Therefore, $V_{GS} = 0$, $I_d = I_{DSS}$ the drain current:

$$V_{DD} - V_{DS} = I_{DSS} R_D$$

The zero bias of fig.a is unique with D-type MOSFET.



2. The voltage divider bias circuit

This circuit can be operated in the enhancement mode or the depletion mode according to the relation between the gate and the source voltage.

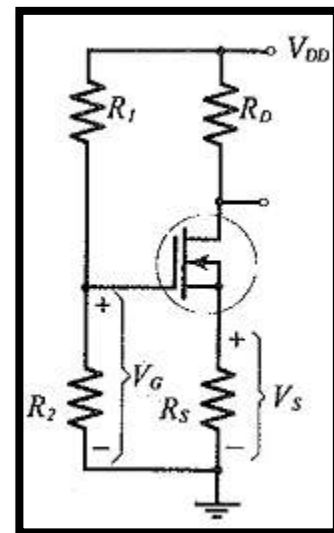
$$V_{GS} = V_G - V_S$$

$$V_G > V_S \quad \text{enhancement mode}$$

$$V_S > V_G \quad \text{depletion mode.}$$

Enhancement mode

$$V_{GS} = + V_G$$



2- Enhancement Type MOSFET (normally OFF mode)

E-MOSFET is a four-terminal device: source(S), gate (G), drain (D) and substrate (Sub.) terminals. The substrate of the MOSFET is in connection with the source terminal thus forming a three-terminal device.

Here, for N channel E-MOSFET V_G must be positive.

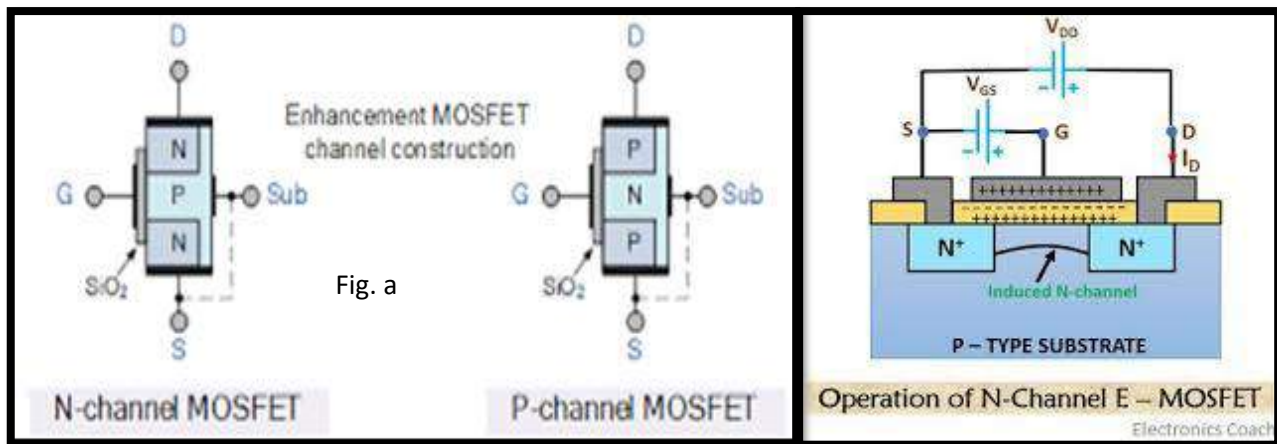
V_{GS} must be $\gg V_{GS(th)}$ for current flow.

Transconductance equation is :

$$I_D = k (V_{GS} - V_{GS(th)})^2$$

A/ Construction

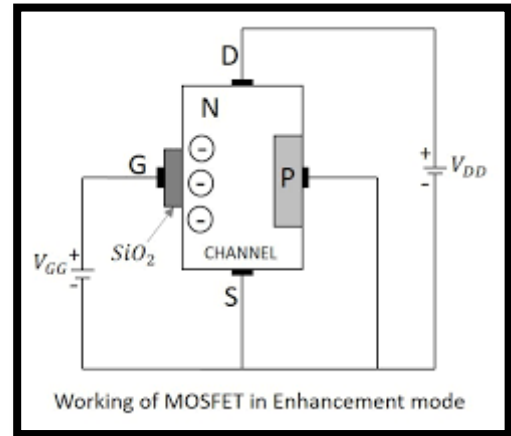
Fig. a shows the construction of E-MOSFET. It shows the normal biasing polarities. As seen the substrate extends all the way to the insulating layer, there is no N-channel, no connection between the drain and the source. When gate voltage is zero, the V_{DD} supply tries to force free electrons to flow from the source to drain, but the P substrate has only a few thermally produced free electrons. As a result, the drain current is almost zero. **The E- MOSFET is a normally OFF.**



B/ Operation

When V_{GS} is positive ($V_{GS} > 0$), the gate attracts free electrons into the P-substrate region. These free electrons recombine with the holes in the p-substrate near the silicon dioxide layer.

When V_{GS} is large enough, all these holes near the silicon dioxide layer are with electrons and the free electrons then acts as a channel between

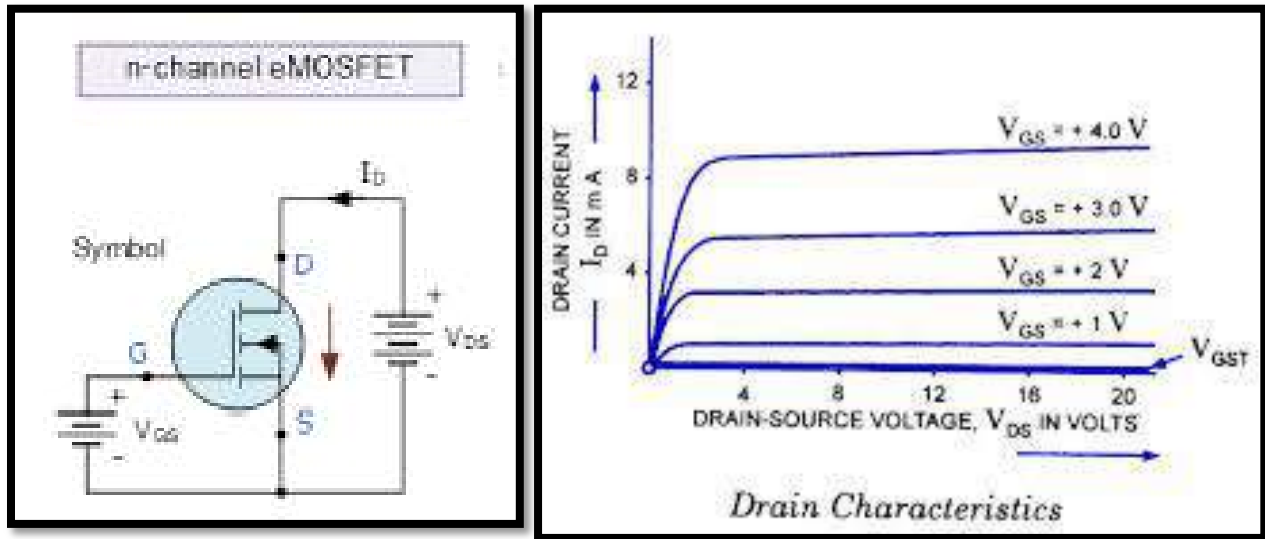


the drain and the source electrons start flowing from source and drain. This layer will become N-type because of the induced free electrons. The effect is as though an N-type layer between the source and drain has been created (a channel has been induced). **This N-type layer is known as n-type inversion layer or induced channel.**

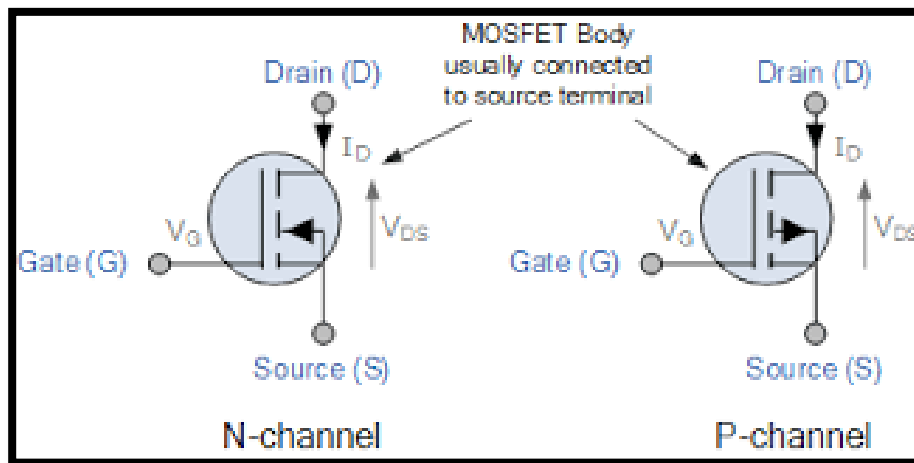
This E-MOSFET is called the N induced channel E-MOSFET. When this layer is formed, the terminal is turned on and free electrons can easily flow from the source to drain. The minimum value of gate to source voltage V_{GS} which can create inversion layer is known as **gate threshold gate voltage $V_{GS(th)}$.**

Thus, the transistor is off when $V_{GS} < V_{GS(th)}$ and is on, when $V_{GS} > V_{GS(th)}$. Thus the conducting capability of enhancement type MOSFET depends on the action of N-type inversion layer.

The same can be said about the E-MOSFET where the drain and the source are of P-type semiconductor, the substrate will be of N-type semiconductor but of course the channel will a P-induced layer. **What must the polarity of the voltage on the gate be?**



C/Symbol



D/ Characteristics

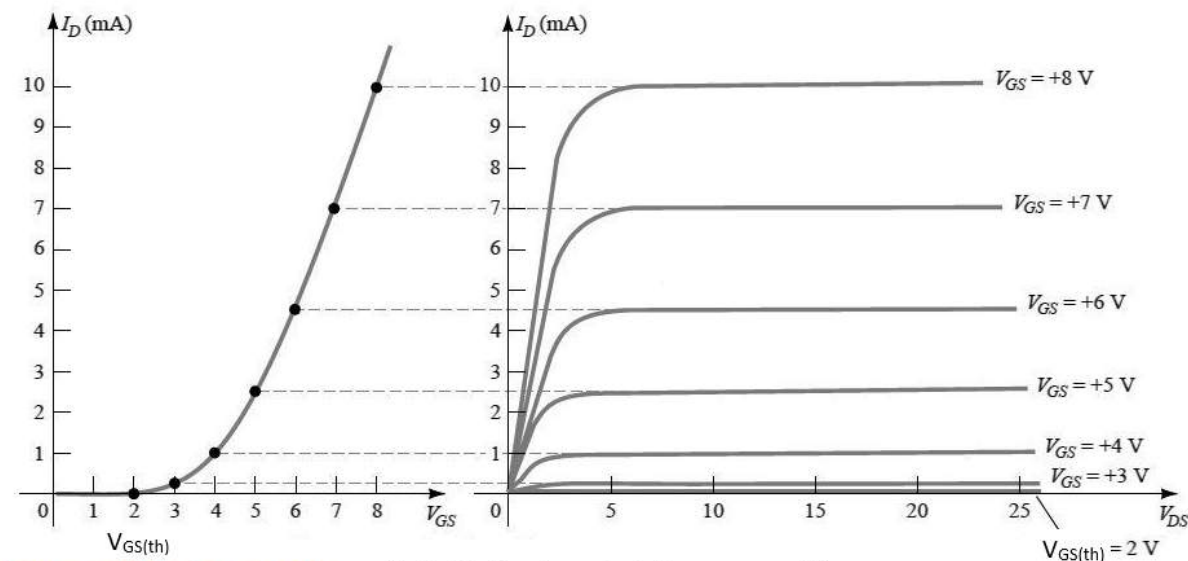
For $V_{GS} < V_{GS(th)}$ $I_D = 0$.

The characteristic curves start for $V_{GS} > V_{GS(th)}$. As V_{GS} increases the drain current increases. For a certain value of V_{GS} , three regions are noticed: the ohmic region, the saturation region and the breakdown region (not drawn in the figure, which happens when the values of V_{DS} and V_{GS} exceeds the values that the

MOSFET can stand. These voltages values will result in the destruction of the insulating layer).

From these curves, the transconductance curve can be drawn, which shows the relation between I_d and V_{GS} . The equation of this curve is:

$$I_d = k (V_{GS} - V_{GS(th)})^2 \text{ where } K \text{ is a constant}$$



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Fig.3-34: the characteristic curves and the transconductance curve of the common drain E-MOSFET

E/ Biasing

1) Drain feedback bias, Fig. a, a type of bias that you can use only with enhancement type MOSFETs. When the MOSFET is conducting, it has a drain current $I_{d(on)}$ and a drain voltage of $V_{DS(on)}$. Since the gate current is approximately zero.

$$V_G = V_D$$

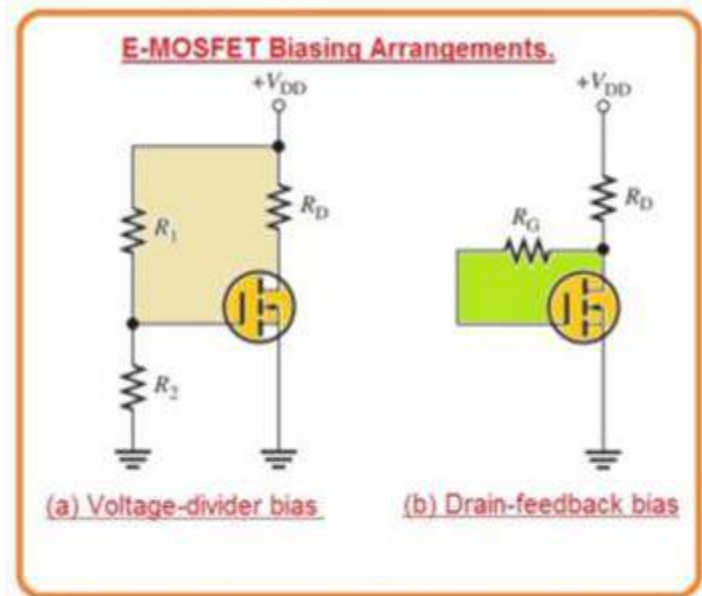
$$V_{DD} - V_D = I_D R_D$$

$$V_{DD} - V_G = I_D R_D$$

2- Voltage divider bias circuit

Fig,b

$$V_G = V_{R2}$$

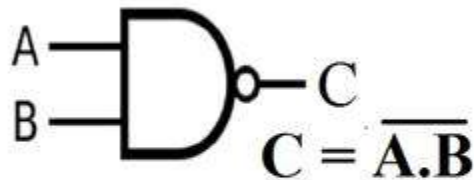


The Universal Property of NAND and NOR Gates

The NAND Gate as a Universal Logic Element

The NAND gate is a **universal gate** because it can be used to produce the NOT, the AND, the OR, and the NOR functions. An inverter can be made from a NAND gate by connecting all of the inputs together and creating, in effect, a single input.

NAND GATE

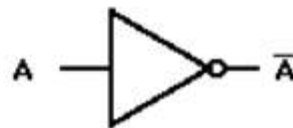


Truth Table

INPUT		OUTPUT
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

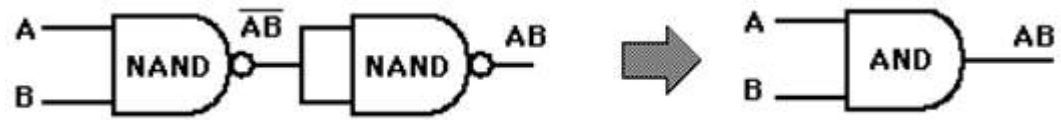
1- NAND gate as NOT gate

$$\overline{A \cdot A} = \overline{A}$$



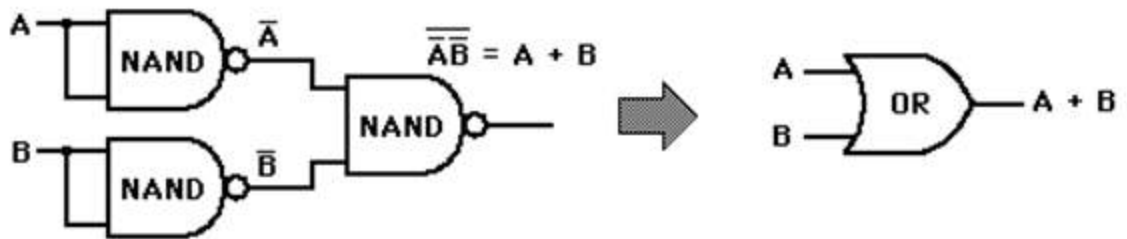
2- NAND gate as AND gate

$$Y = \overline{\overline{AB} \overline{AB}} = \overline{\overline{AB}} \cdot \overline{\overline{AB}} = AB$$



3- NAND gate as OR gate

$$\overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$$



H.W.: In a similar manner, it can be shown that NOR gates can be arranged to implement any of the Boolean operations.

Q1/ N-channel JFET in a self-biased circuit $I_{DD5}=1.65\text{mA}$, $V_{GS(OFF)}=-2\text{V}$, $V_{DD}=24\text{V}$.
It is desired to bias at $I_d=0.8\text{mA}$. Find the values of V_{GS} , R_s , g_m .

Sol.

$$1- \frac{I_d}{I_{DD5}} = \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2$$

$$\frac{0.8\text{mA}}{1.65\text{mA}} = \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2$$

$$0.4848 = \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]^2 \quad (\text{نجدز الطرفين})$$

$$0.696 = 1 - \frac{V_{GS}}{-2}$$

$$V_{GS} = -0.607\text{V}$$

$$2- V_{GS} = -I_D R_s$$

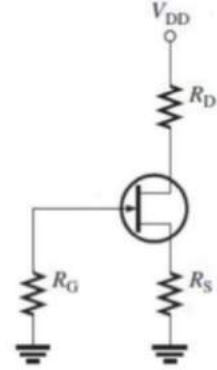
$$R_s = -\frac{V_{GS}}{I_d} = -\frac{-0.607\text{V}}{0.8\text{mA}}$$

$$R_s = 758.75\Omega$$

$$3- g_m = \frac{-2I_{DD5}}{V_{GS(OFF)}} \left[1 - \frac{V_{GS}}{V_{GS(OFF)}} \right]$$

$$= -\frac{2 \times 2 \times 1.65\text{mA}}{-2\text{V}} \left[1 - \frac{-0.607\text{V}}{-2\text{V}} \right]$$

$$g_m = 2.29845\text{mA/V}$$



Q2/ Design a self-biased circuit of N-channel JFET at $I_d=1.6\text{mA}$, $V_{GS}=-3\text{V}$, $V_{DD}=18\text{V}$, $V_{DS}=10\text{V}$.

$$V_{GS}=V_G-V_S$$

$$= 0 - I_d R_S$$

$$R_S = -\frac{V_{GS}}{I_d} = 1.8\text{K}\Omega$$

$$V_{DD}=I_d(R_S+R_D)+V_{DS}$$

$$18\text{V} = 1.6\text{mA} (R_S+R_D) + 10\text{V}$$

$$(R_S+R_D)= 5\text{K}\Omega$$

$$R_D = 3.2\text{K}\Omega$$

