Advanced Computer Architecture

2020-2021

المرحلة الثالثة / الفصل الاول

أستاذ المادة

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Intel 80386 MP architecture:

The 80386 is a high performance 32-bit microprocessor designed to drive the most advanced computer-based applications. The 80386 forms the basis for a high-performance 32-bit system. The 80386 incorporates multitasking support, memory management, pipelined architecture, address translation caches, and a high-speed bus interface all on one chip.

The 80386 features 32-bit wide internal and external data paths and eight general-purpose 32-bit registers. The instruction set offers 8-, 16-, and 32-bit data types, and the processor outputs 32-bit physical addresses directly, for a physical memory capacity of four gigabytes.

Pipelined architecture enables the 80386 to perform instruction fetching, decoding, execution, and memory management functions in parallel

The internal architecture of the 80386 consists of six functional units that operate in parallel. Fetching, decoding, execution, memory management, and bus accesses for several instructions are performed simultaneously. This parallel operation is called pipelined instruction processing. With pipelining, each instruction is performed in stages, and the processing of several instructions at different stages may overlap as illustrated in Figure 1. The six-stage pipelined processing of the 80386 results in higher performance and an enhanced throughput rate over non-pipelined processors. The six functional units of the 80386 are identified as follows; Figure 2 shows the organization of these units.

• Bus Interface Unit

• Code Prefetch Unit

• Instruction Decode Unit

• Execution Unit

• Segmentation Unit

• Paging Unit

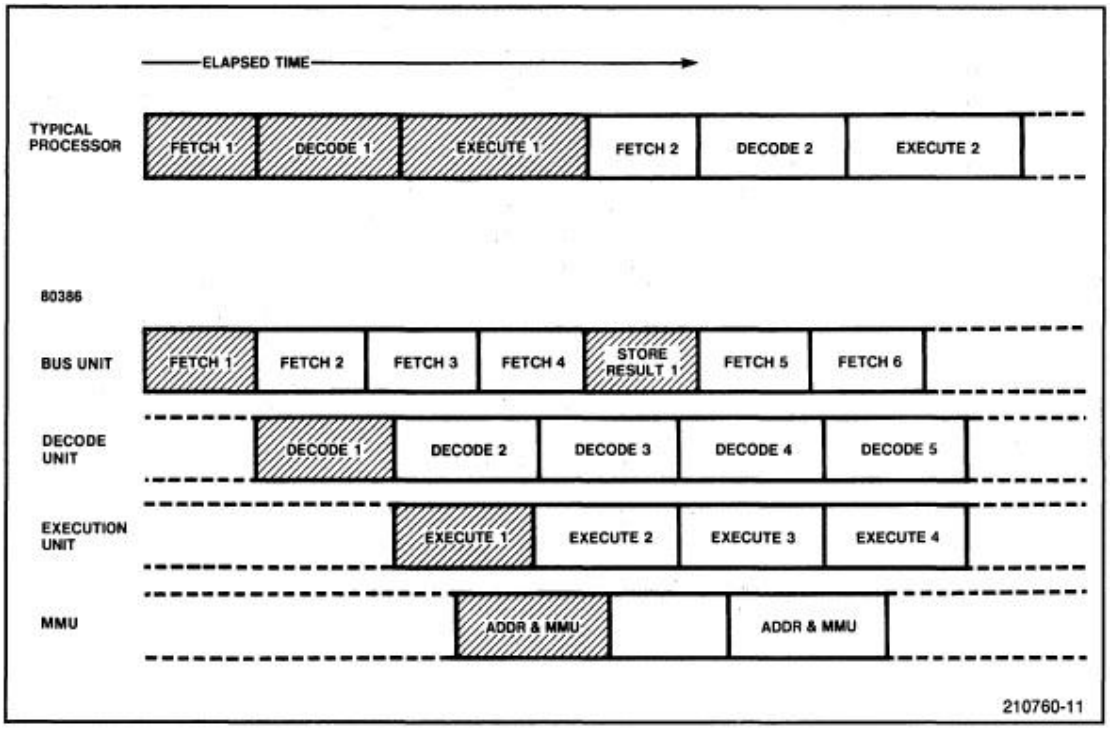

Figure 1 **Instruction Pipelining**

1- BUS INTERFACE UNIT

The Bus Interface Unit provides the interface between the 80386 and its environment. It accepts internal requests for code fetches (from the Code Prefetch Unit) and data transfers (from the Execution Unit), and prioritizes the requests. At the same time, it generates or processes the signals to perform the current bus cycle. These signals include the address, data, and control outputs for accessing external memory and I/O. The Bus Interface Unit also controls the interface to external bus masters and coprocessors.

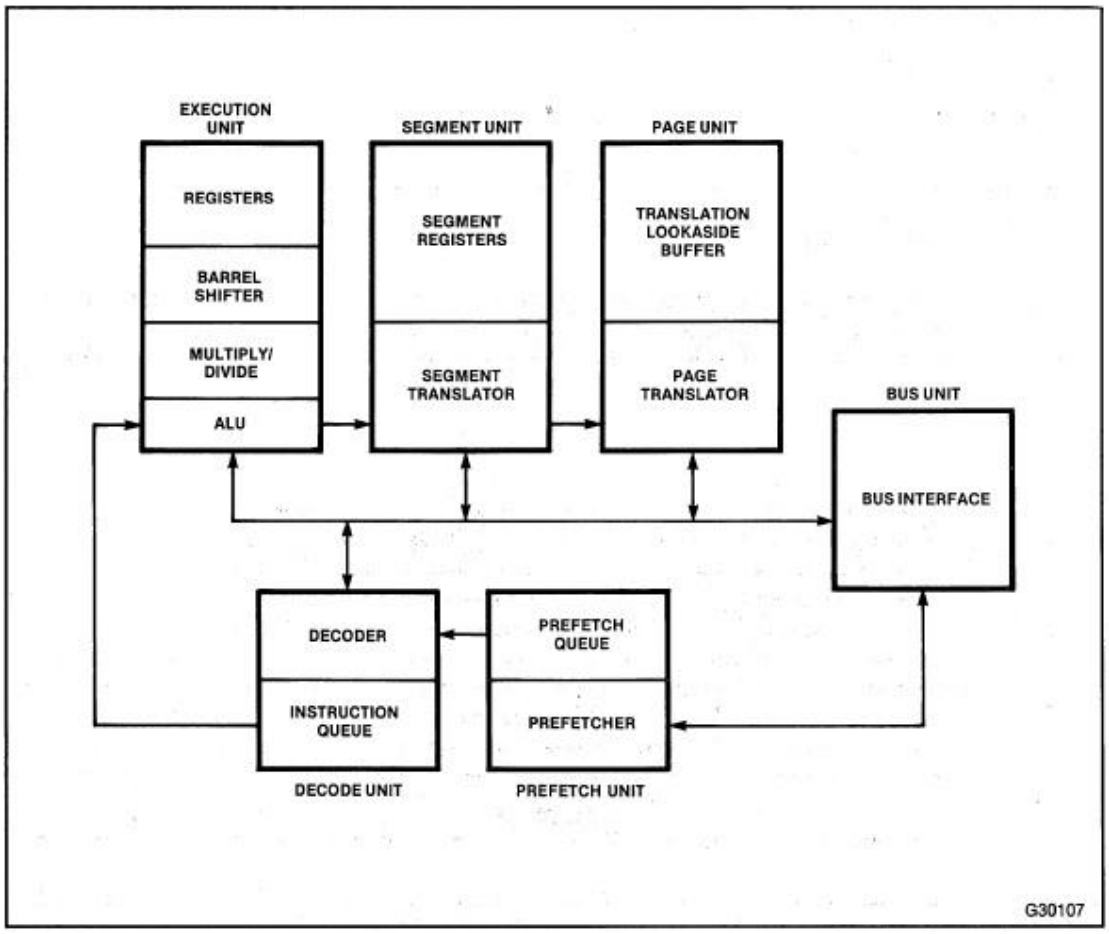

Figure 2 Intel 80386 Functional Units

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1- CODE PREFETCH UNIT

The Code Prefetch Unit performs the program look ahead function of the 80386. When the Bus Interface Unit is not performing bus cycles to execute an instruction, the Code Prefetch Unit uses the Bus Interface Unit to fetch sequentially along the instruction byte stream. These prefetched instructions are stored in the 16-byte Code Queue to await processing by the Instruction Decode Unit. Code prefetches are given a lower priority than data transfers; assuming zero wait state memory access, prefetch activity never delays execution. On the other hand, if there is no data transfer requested, prefetching uses bus cycles that would otherwise be idle. Instruction prefetching reduces to practically zero the time that the processor spends waiting for the next instruction.

2- INSTRUCTION DECODE UNIT

The Instruction Decode Unit takes instruction stream bytes from the Prefetch Queue and translates them into microcode. The decoded instructions are then stored in a three-deep Instruction Queue (FIFO) to await processing by the Execution Unit. Immediate data and opcode offsets are also taken from the Prefetch Queue.

3- EXECUTION UNIT

The Execution Unit executes the instructions from the Instruction Queue and therefore communicates with all other units required to complete the instruction. The functions of its three subunits are as follows:

• The Control Unit contains microcode and special parallel hardware that speeds multiply, divide, and effective address calculation.

• The Data Unit contains the ALU, a file of eight 32-bit general-purpose registers, and a 64-bit barrel shifter (which performs multiple bit shifts in one clock). The Data Unit performs data operations requested by the Control Unit.

• The Protection Test Unit checks for segmentation violations under the control of the microcode. To speed up the execution of memory reference instructions, the Execution Unit partially overlaps the execution of any memory reference instruction with the previous instruction. Because memory reference instructions are frequent, a performance gain of approximately nine percent is achieved.

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SEGMENTATION UNIT

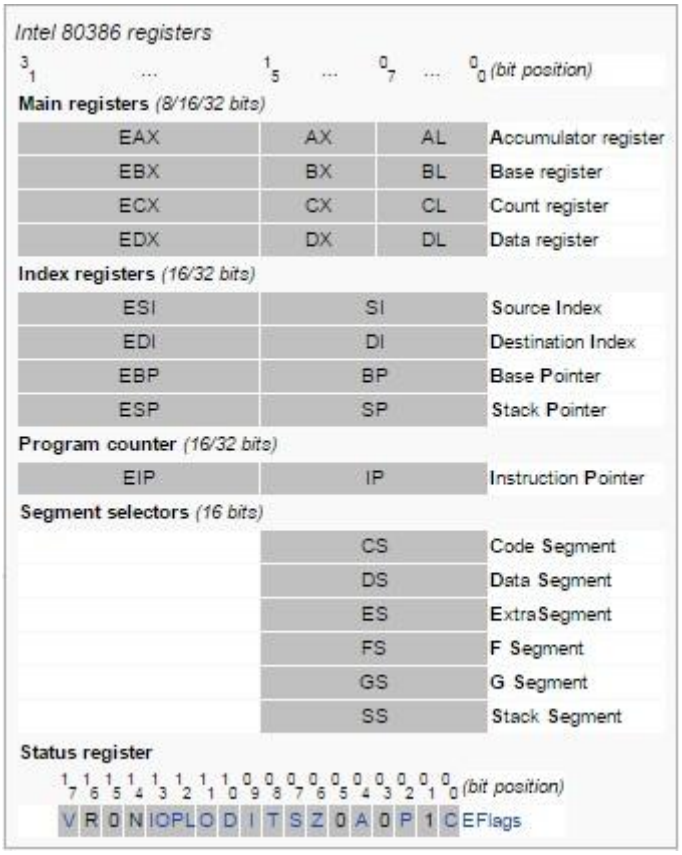
The Segmentation Unit translates logical addresses into linear addresses at the request of the Execution Unit. The on-chip Segment Descriptor Cache stores the currently used segment descriptors to speed this translation. At the same time it performs the translation, the Segmentation Unit checks for bus-cycle segmentation violations. (These checks are separate from the static segmentation violation checks performed by the Protection Test Unit.) The translated linear address is forwarded to the Paging Unit.

PAGING UNIT

When the 80386 paging mechanism is enabled, the Paging Unit translates linear addresses generated by the Segmentation Unit or the Code Prefetch Unit into physical addresses. (If paging is not enabled, the physical address is the same as the linear address, and no translation is necessary.).

The Paging Unit forwards physical addresses to the Bus Interface Unit to perform memory and I/O accesses.

Intel 80386 mp registers:



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Intel 80386 MP Processing Modes

The processing mode of the 80386 determines the features that are accessible. The 80386 has three processing modes:

1. Real-Address Mode.
2. Virtual 8086 Mode.
3. Protected Mode.

- Real-address mode (often called just "real mode") is the mode of the processor immediately after RESET. In real mode the 80386 appears to programmers as a fast 8086 with some new instructions. Most applications of the 80386 will use real mode for initialization only.

- Virtual 8086 mode (also called V86 mode) is a dynamic mode in the sense that the processor can switch repeatedly and rapidly between V86 mode and protected mode. The CPU enters V86 mode from protected mode to execute an 8086 program, then leaves V86 mode and enters protected mode to continue executing a native 80386 program.

- Protected mode is the natural 32-bit environment of the 80386 processor. In this mode all instructions and features are available.

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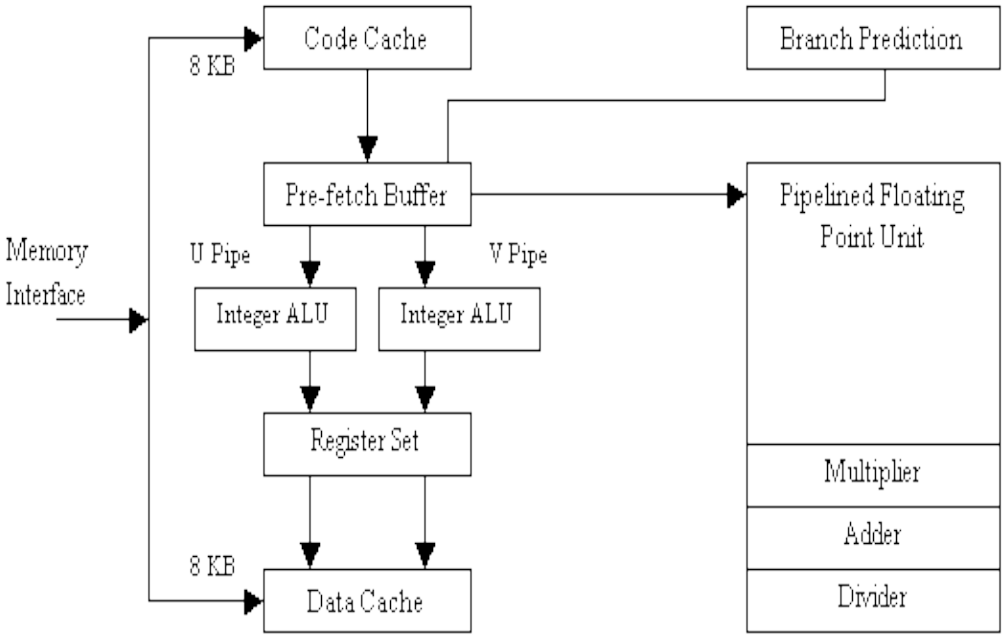
Intel 80486 MP architecture:

- The 32-bit 80486 is the next evolutionary step up from the 80386.
- One of the most obvious feature included in an 80486 is a built in math coprocessor. This coprocessor is essentially the same as the 80387 processor used with a 80386, but being integrated on the chip allows it to execute math instructions about three times as fast as a 80386/387 combination.
- 80486 is an 8Kbyte code and data cache.



- The memory system for the 486 is identical to 386 microprocessor. The 486 contains 4G bytes of memory beginning at location 00000000H and ending at FFFFFFFFH.
- The major change to the memory system is internal to 486 in the form of 8K byte cache memory, which speeds the execution of instructions and the acquisition of data.
- The 80486 contains the same memory-management system as the 80386.

The Floating Point Unit

The Intel Architecture Floating-Point Unit (FPU) provides high-performance floating-point processing capabilities. It supports the real, integer, and BCD-integer data types. The FPU executes instructions from the processor's normal instruction stream and greatly improves the efficiency of Intel Architecture processors in handling the types of high-precision floating-point processing operations commonly found in scientific, engineering, and business applications.

The architecture of the Intel Architecture FPU has evolved in parallel with the architecture of early Intel Architecture processors. The first Intel Math Coprocessors (the Intel 8087, Intel 287, and Intel 387) were companion processors to the Intel 8086/8088, Intel 286, and Intel386 processors, respectively, and were designed to improve and extend the numeric processing capability of the Intel Architecture. The Intel486 DX processor for the first time integrated the CPU and the FPU architectures on one chip. The Pentium processor's FPU offered the same architecture as the Intel486 DX processor's FPU, but with improved performance. The Pentium Pro processor's FPU further extended the floating-point processing capability of Intel Architecture family of processors and added several new instructions to improve processing throughput.

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Intel Pentium Processor

The Pentium microprocessors have advanced superscalar, the *superscalar factor* (the maximum number of instructions that can be completed in a clock cycle) is three in the Pentium Pro processor. And the data path width inside the Pentium Pro is 64-bits. Figure 1 shows functional block diagram of the Pentium Pro processor micro architecture.

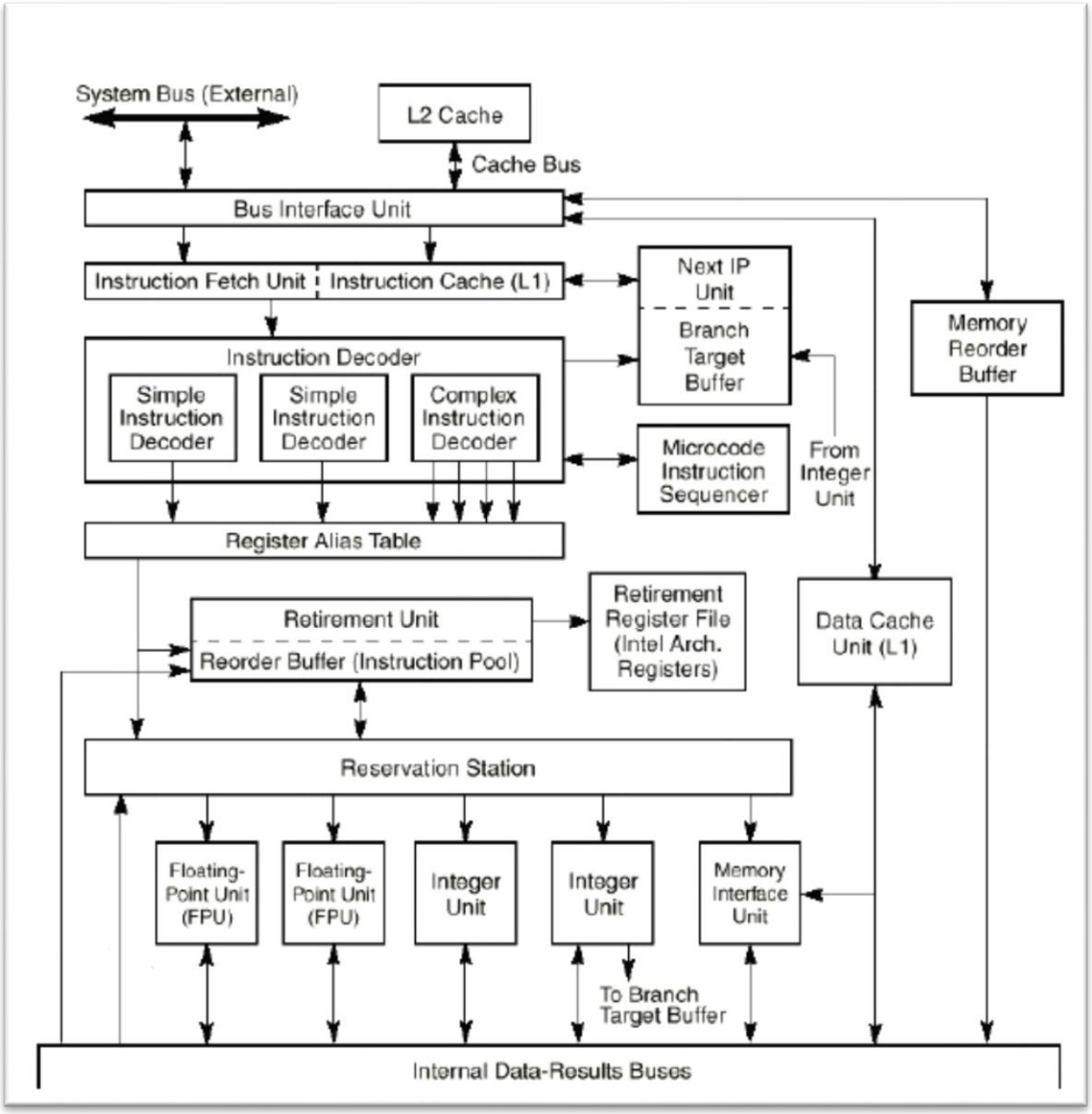

Figure 1: Functional block diagram of Pentium Pro processor

Referring to the above diagram, we can divide the architecture into four processing units and the memory subsystem as follows:

- Memory subsystem: This consists of, system bus, L2 cache, bus interface unit, instruction cache (L1), data cache unit (L1), memory interface unit, and memory reorder buffer.
- Fetch/Decode unit: This unit comprises of instruction fetch unit, branch target buffer, instruction decoder, microcode sequencer, and register alias table.
- Instruction pool: This is made up of the reorder buffer
- Dispatch/Execute unit: This has a reservation station, two integer units, two floating-point units, and two address generation units.
- Retire unit: This consists of the retire unit and retirement register file.

These processing units are discussed in little more detail in the following subsections.

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Memory Subsystem

The memory subsystem for the Pentium Pro processor consists of main system memory, the primary cache (L1), and the secondary cache (L2). The bus interface unit accesses system memory through the external system bus. The external system bus is a 64-bit bus that handles each bus access as separate request and response operations (transaction oriented bus). While the bus interface unit is waiting for a response to one bus request, it can issue numerous additional requests. The bus interface unit accesses the L2 cache through a 64-bit cache bus. This bus is also transactional oriented, supporting up to four concurrent cache accesses, and operates at the full clock speed of the processor. Bus interface unit gets access to the L1 caches is through internal buses. Processor's execution units request memory through the memory interface unit and the memory order buffer.

These units have been designed to support a smooth flow of memory access requests through the cache and system memory hierarchy to prevent memory access blocking. The L1 data cache automatically forwards a cache miss on to the L2 cache. Memory requests to the L2 cache or system memory go through the memory reorder buffer. The memory reorder buffer functions as a scheduling and dispatch station. This unit keeps track of all memory requests and is able to reorder some requests to prevent blocks and improve throughput.

The Fetch/Decode Unit

The fetch/decode unit reads instructions from the L1 instruction cache and decodes them into a series of micro-operations (micro-ops). This micro-op stream is then sent to the instruction pool. From the instruction cache the instruction fetch unit fetches one 32-byte cache line per clock. It marks the beginning and end of the instructions in the cache lines and transmits 16 aligned bytes to the decoder. The instruction decoder contains three parallel decoders:

- two simple-instruction decoders
- one complex instruction decoder.

Each decoder converts an instruction into one or more triadic micro-ops (two logical sources and one logical destination per micro-op). Micro-ops are primitive instructions that are executed by the processor's six parallel execution units. Many instructions are converted directly into single micro-ops by the simple instruction decoders, and some instructions are decoded into from one to four micro-ops. The more complex instructions are decoded into sequences of preprogrammed micro-ops obtained from the microcode instruction sequencer.

The processor provides 40 internal, general-purpose registers, which are used for the actual computations. These registers can handle both integer and floating point values. The enqueued micro-ops from the instruction decoder are sent to the register alias table unit, where references to the logical architecture registers are converted into internal physical register references. Then the allocator in the register alias table unit adds status bits and flags to the micro-ops to prepare them for out-of-order execution and sends the resulting micro-ops to the instruction pool.

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Instruction Pool (Reorder Buffer)

The reorder buffer is an array of content-addressable memory, arranged into 40 micro-op registers. It contains micro-ops that are waiting to be executed, as well as those that have already been executed but not yet committed to machine state. The dispatch/execute unit can execute instructions from the reorder buffer in any order.

Dispatch/Execute Unit

The dispatch/execute unit schedules and executes the micro-ops stored in the reorder buffer according to data dependencies and resource availability. The reservation station handles the scheduling and dispatching of micro-ops from the reorder buffer. The results of a micro-op execution are returned to the reorder buffer and stored along with the micro-op until it is retired. If two or more micro-ops of the same type are available at the same time, then the reorder buffer follows a FIFO algorithm to execute them. Two integer units, two floating-point units, and one memory-interface unit handle execution of micro-ops. Thus up to five micro-ops can be scheduled per clock. The two integer units can handle two integer micro-ops in parallel. The memory interface unit handles the load and store micro-ops. The memory interface unit executes both a load and a store in parallel in one clock cycle. The floating-point execution units are similar to those found in the Pentium processor, few new floating-point instructions have been added to the Pentium Pro processor.

Retirement Unit

The retirement unit commits the results of speculatively executed (decided by branch prediction mechanism) micro-ops to permanent machine state and removes the micro-ops from the reorder buffer. The retirement unit continuously checks the status of micro-ops in the reorder buffer, similar to the reservation buffer. It then retires completed micro-ops in their original program order. The retirement unit can retire three micro-ops per clock. In retiring a micro-op. After the results have been committed to machine state, the micro-op is removed from the reorder buffer.

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Instruction Set Architecture Features

To make a computer hardware work we must speak to the hardware in its language. The words of this machine language are called instructions, and the vocabulary is called an instruction set. The Pentium processor is a CISC (Complex-Instruction-Set-Computer) architecture, but it achieves high performance by using many organizational features of RISC (Reduced-Instruction-Set Computer) architecture.

All the Intel Architecture instructions divided into four major groups:

- integer,
- MMX technology,
- floating-point, and
- system instructions.

Integer Instructions

Integer instructions perform the integer arithmetic, logic, and program flow control operations that programmers commonly use to write application and system software to run on an Intel Architecture processor. The integer instructions include different types of instructions like, data transfer instructions (PUSH, POP, MOV etc.); binary

arithmetic instructions (ADD-integer add, ADC -Add with carry, SUB-Subtract, SBB-Subtract with borrow etc.); Decimal Arithmetic (DAA-Decimal adjust after addition, DAS-Decimal adjust after subtraction, etc.); Logic Instructions (AND, OR, XOR, NOT); Shift and Rotate Instructions (SAR-Shift arithmetic right, SHR-Shift logical right, etc.)

MMX™ Technology Instructions

The MMX instructions execute on those Intel Architecture processors that implement the Intel MMX technology. These instructions operate on packed-byte, packed-word, packed-doubleword, and quadword operands. All of the MMX technology instructions are grouped as MMX™ Conversion Instructions, MMX™ Packed Arithmetic Instructions, MMX™ Comparison Instructions, MMX™ Logic Instructions, MMX™ Shift and Rotate Instructions, or MMX™ State Management.

Floating-Point Instructions

The floating-point instructions are those that are executed by the processor's floating point unit (FPU). These instructions operate on floating-point (real), extended integer, and binary-coded decimal (BCD) operands. These instructions include different types like, Data Transfer (FLD-Load real, FST-Store real, etc.); Basic Arithmetic (FADD-Add real, FADDP-Add real and pop, etc.); Comparison (FCOM-Compare real, FCOMP Compare real and pop, etc.)

System Instructions

These instructions are used to control those functions of the processor that are provided to support for operating systems and executives.

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Intel Pentium III Processor

The Pentium III is essentially a Pentium II running at higher speed, with two interesting and useful features:

- The processor serial number and
- Streaming SIMD Extensions (SSE).

The processor serial number (or chip ID) is a unique identifier 'burned' into the Pentium III processor that can be accessed over the internet, allowing e-commerce sites and others to know which machine is visiting a site or using a service. This has drag Intel Inc to a major controversy. But Intel claims that processor serial number can add value to a wide range of applications in both business and consumer computing. The advantages that the processor serial number can provide are discussed below.

- Security: The e-commerce depends on the assurance that only the authorized people access the confidential information. Applications that take advantage of the processor serial number can use that as another element of identification thus increasing confidentiality. Similarly, processor serial number can strengthen the data security for the consumer web sites who wants to maintain a section open only to their family members or so. It can also be used in businesses for adding a level of validation to electronic signature approvals.

- Manageability: IT departments use various ways to track assets such as MAC address or BIOS's GUID. But Intel claims that all these could be erased, so less reliable. But, processor serial number can be reliably used as a once it is burn on the chip at the time of manufacture it can never be erased. So designing applications using chip ID can help IT customers to manage their resources more efficiently.

- Information Management: Companies can turn information into a competitive advantage if they can manage it effectively. Information related applications can use processor serial numbers to handle tasks ranging from finding multiple copies of virus-infected document, tracking change information, to delivering customized information to the end user.

The other significant feature of the Pentium processor is the Streaming SIMD Extensions (SSE). Usually, the processors are SISD meaning Single Instruction and Single Data thus processing one data in one instruction. MMX and SSE, both share the concept of SIMD, they differ in the type of data they handle, and the way they are supported in the processor. MMX instructions are SIMD for integers, while SSE instructions are SIMD for single-precision floating-point number. MMX instructions operate on two 32-bit integers simultaneously, while SSE instructions operate on four 32- bit floats simultaneously. A major difference between MMX and SSE is that no new registers were defined for MMX, while eight new registers have been defined for SSE. The SSE can be used in 3D graphics applications.